Microstructural Examination of Extended Crystal Defects in Silicon Selective Epitaxial Growth

H. YEN,* E.P. KVAM,* R. BASHIR,† and G.W. NEUDECK†

*School of Materials Engineering, School of Electrical Engineering,† Purdue University, West Lafayette, IN 47907

Selective epitaxial growth has been used to produce electronically isolated devices. The oxide/silicon interfaces in such materials are often associated with regions of poor device performance. In this study, the extended defects in the bulk near interfacial regions are examined by transmission electron microscopy. Process modifications suggest a large portion of the defects were due to thermal expansion mismatch and can be avoided.

Key words: Oxide/silicon interfaces, thermal expansion mismatch, TEM

INTRODUCTION

The growth of electronically isolated high quality silicon epilayers by selective epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO) processes has been recognized as an important goal for several years.[1,2] However, various processing defects have commonly been observed in these materials.[3–5] Those defects present in the active device area can cause functionality failures, excessive leakage current, or mobility reduction. Any reduction in the crystal defect density in the device active area would be beneficial in terms of circuit performance improvement and yield increase. In this work, transmission electron microscopy (TEM) was used to observe defects in epilayers and to characterize these defects. Two specific structures were examined: a deep trench SEG device, and a novel 2-D confined ELO structure. Transmission electron microscopy observation showed that defects could in some instances be tremendously reduced by alterations in the fabrication process.

The structures examined are shown schematically in Fig. 1. The basic SEG process simply involves opening a seed hole through a surface oxide layer to uncover the bare Si substrate, and using this exposed Si as the epitaxial growth surface. The selectivity comes in that (ideally) no growth occurs directly onto the oxide regions. To examine more carefully the oxide sidewall effects during SEG, a deep trench structure was utilized to maximize the sidewall area. This structure is shown in Fig. 1a.

An ELO structure is actually an extension and continuation of the SEG process beyond the top of the oxide surface, both above and across the oxide; this is shown in Fig. 1b. As the ELO shows laterally across the oxide surface, two problems have been observed to develop. First, the Si continues to grow upward at approximately the same rate as it grows laterally, hence chemical mechanical polishing is required to planarize the ELO region back to the oxide surface. This also avoids any corner facets and their effects. Second, far away from the seed window edge are regions of oxide which, when reached by the ELO Si growth front, are more likely to induce defects caused by surface roughness and oxide degradation.

A recent novel variation of the ELO process is confined lateral selective epitaxial growth (CLSEG),[6] or 'tunnel epi.'[7] This structure is shown schematically in Fig. 1c. In this process, a hollow enclosed cavity is formed above the SEG seed hole by use of a sacrificial amorphous Si layer, which is deposited in the form the cavity is to take. This layer is then slightly oxidized (which also crystallizes the Si, forming poly) and covered with Si_3N_4 for strength. An access hole is

(Received April 27, 1993; revised July 2, 1993)

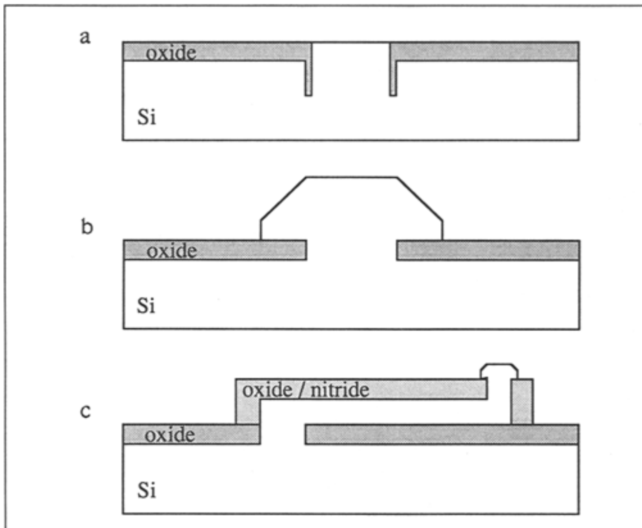


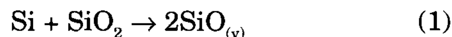
Fig. 1. Schematic cross-sectional views of three basic SEG structures: a deep trench structure (top), a simple ELO growth (middle), and a confined ELO, or CLSEG (bottom).

opened opposite the original substrate seed hole, and the polysilicon is removed with a KOH-based selective etchant. Surprisingly, the growth of SEG Si within the open cavity has been found to be nearly identical to that in conventional geometries.[6] The oxide-lined nitride cavity has the effect of constraining the ELO growth to form broad, shallow SOI layers, thus eliminating further process steps, such as the polishing away of protuberances or excess Si thickness which would normally be present.

SELECTIVE EPITAXIAL GROWTH PARAMETERS

The SEG and confined lateral overgrowth samples used in this study were grown on (001) Si substrates in a reduced pressure pancake chemical vapor deposition (CVD) reactor at 970°C using $SiCl_2H_2$, HCl, and H_2 gasses, in a process described previously.[2,6,8,9] Our previous work has shown that although the observed SEG defect density varied slightly from wafer to wafer, the type and location of defects were similar. These defects have generally been characterized only by optical microscopy. Scattered dislocations or dislocation networks, existing mostly in the overgrown (ELO) regions have been commonly observed and described. Planar defects were often found near overgrowth fronts.

Oxide degradation[10] during selective epitaxial growth has also been observed. The decomposition of oxide was increased by addition of silicon-containing gas according to the reaction:



$$Si + SiO_2 \rightarrow 2SiO_{(v)} \quad (1)$$

which results in roughness at the SiO_2 surface. When single crystal silicon growth fronts are grown over roughened SiO_2 to form SOI structures, the perturbations at this interface may serve as the source for defect formation. It can be imagined that the perfect stacking order of atoms is interrupted by this irregular interface, and the crystal imperfections would be readily nucleated from these defect sites. It has been noted that the defect density is frequently substantially higher for the ELO regions farther away from seed windows. Since the greater distance away from seed windows corresponds to a longer growth time (and time of oxide exposure to Si vapor), the polysilicon nucleation and oxide degradation would be inevitably more serious in the regions more distant from seed windows. Although the polysilicon nucleation over SiO_2 has been substantially suppressed by introducing HCl for poly etching in our experiments,[2] the

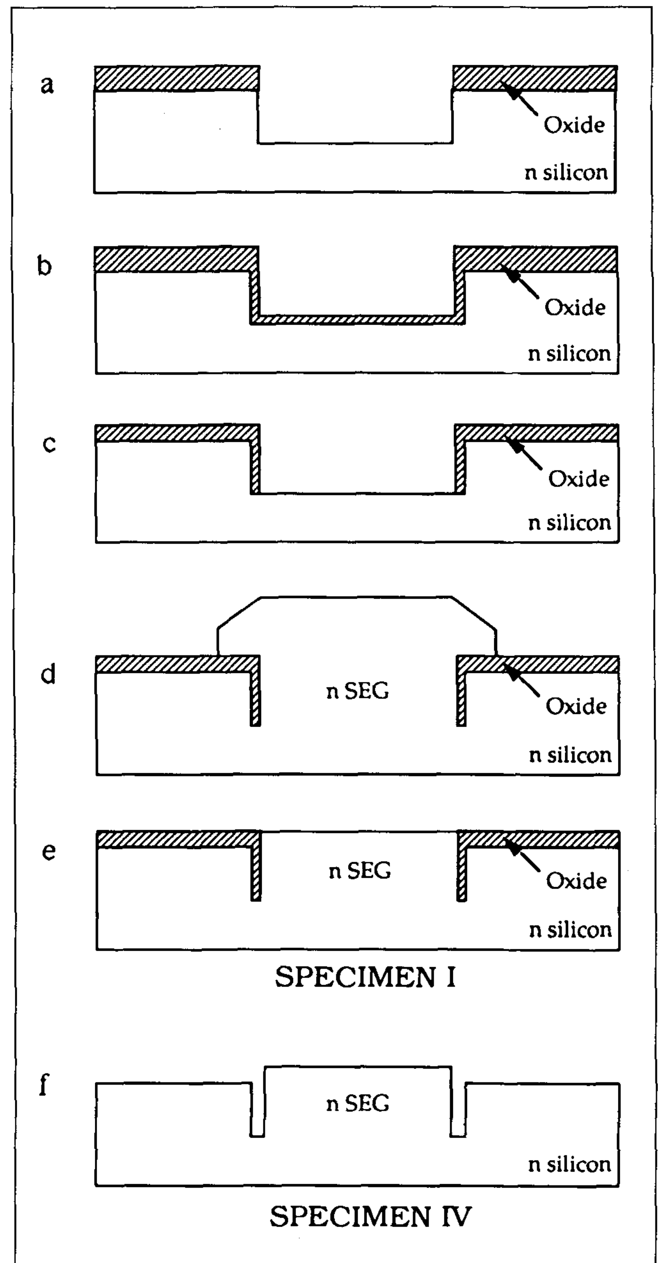


Fig. 2. Schematic diagram of deep trench SEG processing. Oxidized Si is deeply dry-etched (a), then reoxidized (b), and lightly dry-etched (c). The exposed Si is used for epitaxial CVD growth (d), which is planarized to form the deep trench structure (e). For later annealing studies, the SiO_2 walls could be removed by a wet etch (f).

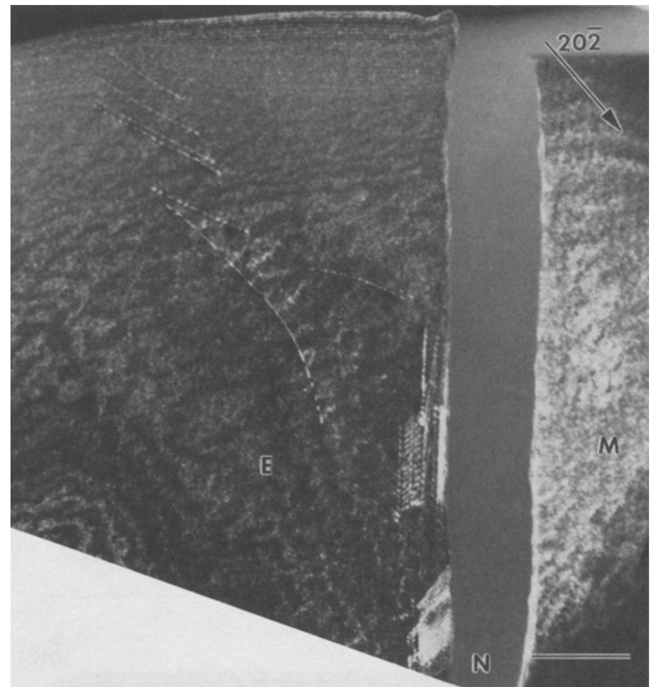
integrity of the oxide layer would still be degraded by dichlorosilane species via reaction.[1]

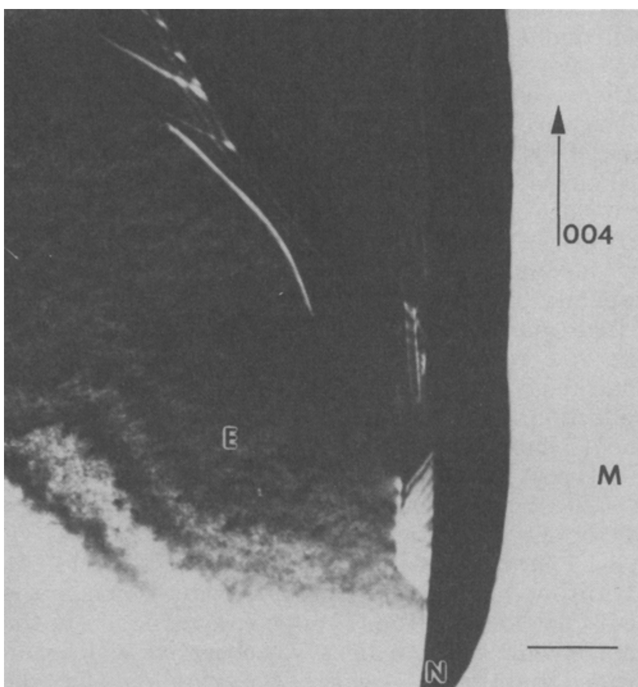
The facet morphology created in the ELO surface imposes further disadvantages to device fabrication, in reducing active device areas and the integrity of metal interconnect lines, and thus usually requires an additional process using chemical-mechanical polishing to planarize the surface. The formation of facets was attributed to the different growth rates along the different crystallographic planes,[11-13] and the relative growth rates of these planes has been examined under different growth parameters. Use of CLSEG structures avoids these complications for device fabrication by eliminating excess upward growth, and reducing the effects of facets. The latter can be further ameliorated by growing through and out of the access hole, as sketched in Fig. 1c, then removing the outgrowth by polishing.

DEFECT REDUCTION BY PROCESSING IMPROVEMENT/SEG TRENCH

We have investigated the defects generated by growth and processing of a SEG deep trench structure. Since SEG defects have been observed mostly near the Si/SiO_2 sidewall interface, a series of experiments was designed to investigate how the defects were generated, and whether they might be avoidable. The deep trench structure maximized the Si/SiO_2 interface area, and also required an oxide wall to terminate at an edge deep in the Si. The oxide wall had a gross aspect ratio of 10 but also narrowed to a sharp point at its base. It was thus, in many ways, a 'worst case' test structure for process-induced defect generation.

The processing sequences, shown schematically in Fig. 2, were as follows. First, a thermal oxide was grown on the n-type substrate. Anisotropic reactive ion etching (RIE) was then used to etch through the oxide and 2.2 μm of silicon. A conformal oxide was subsequently grown at the sidewall and bottom region, and RIE was again applied to open the seed window and expose the silicon only at the bottom. N-





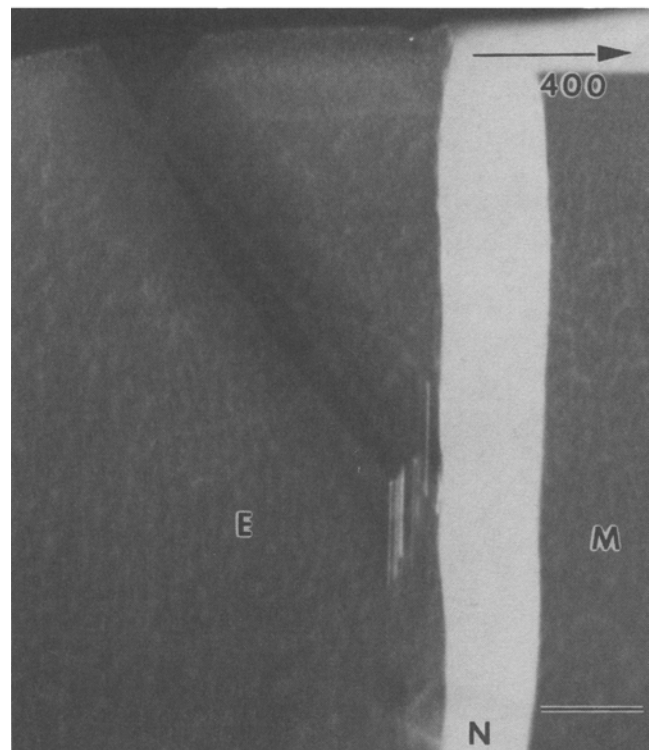


Fig. 3. Three different dark field images from specimen I type process, illustrating dislocations, stacking faults, and a twinned region, the types of defects which were commonly observed in those materials. The main substrate Si is on the right (M), insulating oxide in the middle (N), and epitaxial SEG Si on the left (E). The bar at lower right is 1/4 μm.

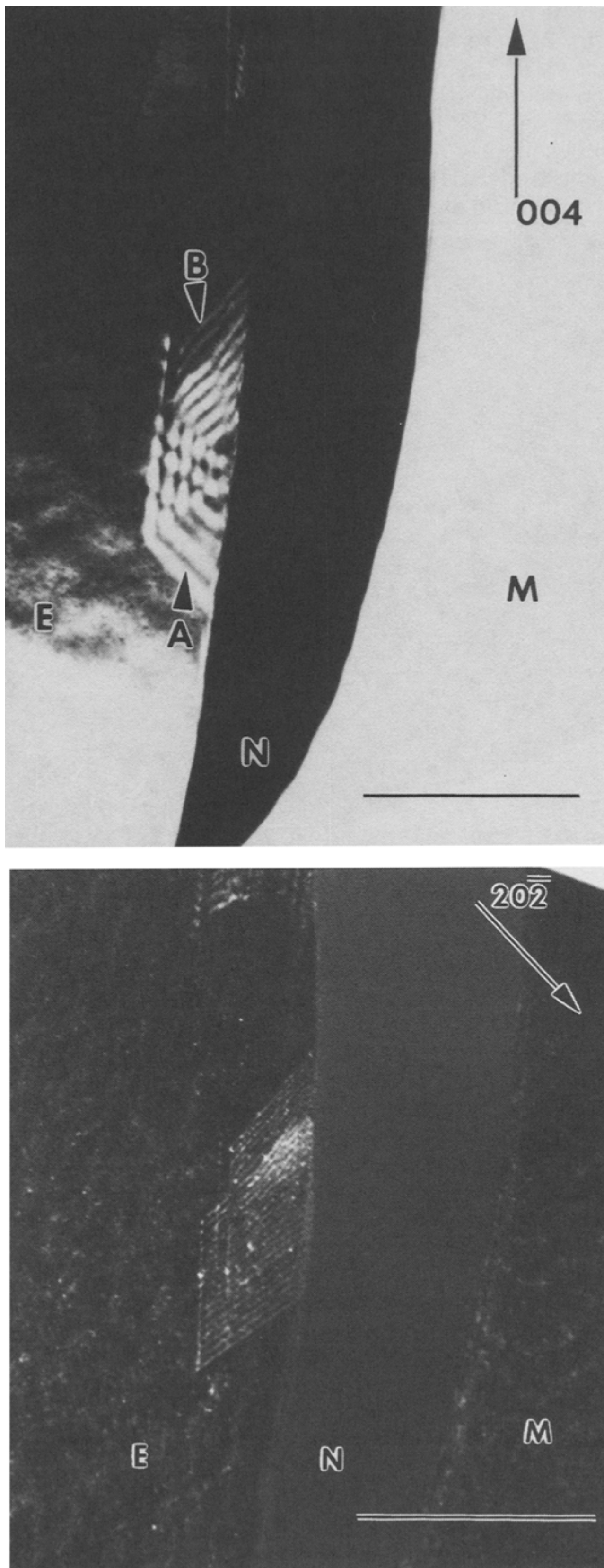


Fig. 4. Dark field images from specimen I process, taken in different region; stacking fault sets initiated at the sidewall can be clearly observed. The main substrate Si is on the right (M), insulating oxide in the middle (N), and epitaxial SEG Si on the left (E). The bar at lower right is 1/4 μm.

type SEG was grown, and followed by chemical-mechanical planarization to polish the top surface. This as-grown specimen, shown schematically in Figs. 1a and 2e, was denoted as specimen I and was used for control purposes. This structure gives the advantage of a large sidewall dimension (about 2.5 μm) of the vertical Si/SiO_2 interface to investigate defect generation. Another specimen, denoted specimen II, was first processed under the same conditions as specimen I, but followed by buffered hydrofluoric acid (BHF) etching to remove the sidewall SiO_2 (thus forming cavities). This temporarily left the SEG Si material as a pedestal free-standing within the trench, as shown schematically in Fig. 2f. A final thermal reoxidation step was than used to grow some SiO_2 in the cavities and on the upper SEG surface.

Figures 3a–3c show TEM micrographs taken from specimen I. All images were taken near the [010] zone axis. Defects were generated mostly within 1 μm of Si/SiO_2 sidewall interface, while a defect-free region was found away from the sidewall in the bulk SEG. Diodes fabricated from these structures corroborated the TEM observations, in that those with active regions near the sidewall were clearly inferior to those in which the active region occupied only the central, defect-free SEG region.[9] Dislocations observed relatively far away from the sidewall were believed to have been driven there by stresses (particularly thermal expansion mismatch, as discussed below). By utilizing various diffracting conditions and two-beam imaging techniques which could render dislocation images out of contrast, the Burgers vectors of the dislocations could be determined. Figures 3a–3c show that all of the dislocations in this region of specimen I are simultaneously visible for the 004 and $20\bar{2}$ reflections, while out of contrast under the 400 (and $31\bar{1}$, not shown here) reflection. By using these and other reflections, it was concluded that these dislocations were of the same type, and had a Burgers vector ±a/2 [011], inclined at 45° to the sidewall.

Pairs of stacking faults originating from the sidewall interface of specimen I were also observed, as shown in Figs. 4a and 4b. The stacking faults were analyzed by viewing the orientation of fringes and using tilting capabilities in TEM. It may be noted that one type of fringe (marked A in Fig. 4a) was out of contrast using the $20\bar{2}$ reflection, while the other type of fringe (marked B in Fig. 4a) was out of contrast using the 202 reflection. This enabled us to determine the displacement vector, R, and the planes of the stacking faults. For type A fringes, the phase factor α vanished under g = $20\bar{2}$ beam; therefore, the possible displacement vector of type A stacking fault was either a/3[111] or a/3[$1\bar{1}1$], and planes of stacking faults (111) or ($1\bar{1}1$). By tilting the specimen from the orientation near the [010] pole toward the [110] pole, a reduction in the image width of the fringes was observed, which confirmed that the ($1\bar{1}1$) was the only candidate for type A stacking faults, and the displacement vector was thus a/3[$1\bar{1}1$]. For type B fringes, the confusion between possible ($\bar{1}11$) and ($\bar{1}\bar{1}1$) planes was also

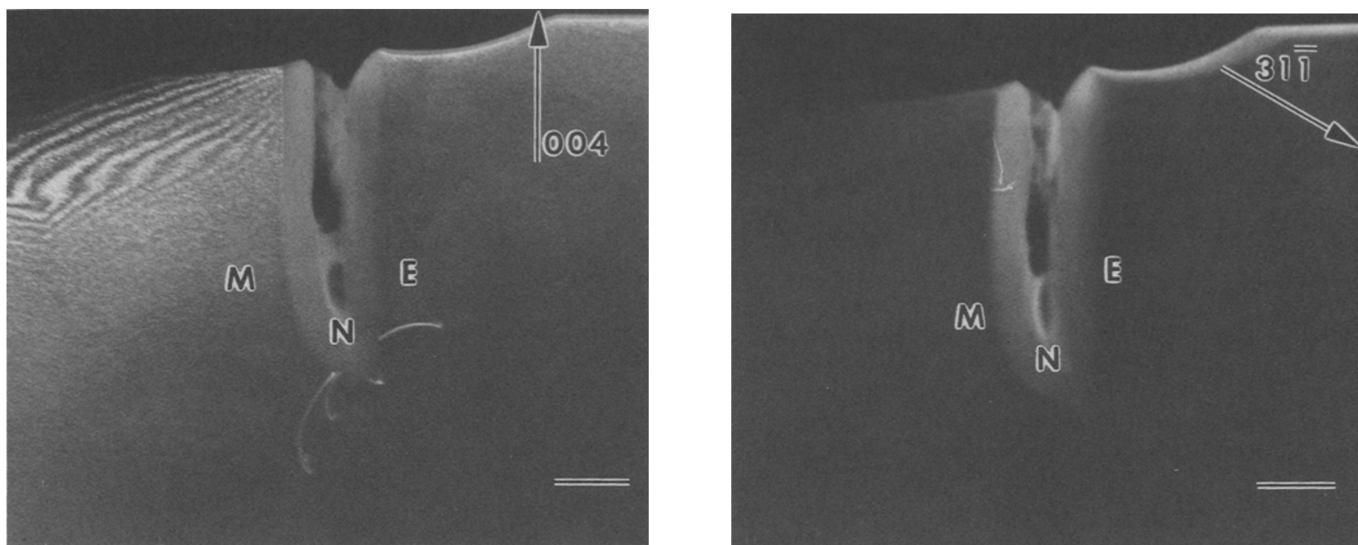


Fig. 5. Weak beam dark field images from a type II specimen; the only defects observed were dislocations emanating from the sharp corner of the sidewall oxide as it terminated deep in the Si. The epitaxial SEG Si on the right (E), insulating oxide in the middle (N), and main substrate Si is on the left (M). The bar at lower right is 1/2 μm.

removed by tilting experiments. By tilting the specimen in the same orientation from the [010] pole to the [110] pole, an increase in the image width of fringes was observed. These type B stacking faults were characterized as having a displacement vector of the form a/3[$\bar{1}\bar{1}1$].

Figures 5a and b show TEM micrographs taken from specimen II. (The oxide formed by thermal reoxidation did not completely fill the cavity region produced by BHF etching of the first thermal oxide, and left some voids in the oxide. To obtain the highest quality device, an increase in reoxidation time would probably be needed to remove the voids and improve the integrity of the SiO_2 structure.) An obvious reduction of defects was observed in specimen II. Lattice dislocations, the sole defects observed in specimen II, were found only at the sharp end of the sidewall interface, and propagated from this point into both the epilayer and the substrate. This differed from the observations of specimen I, where dislocations and other defects were found in the epilayer along the sidewall. The dislocation images nearly vanished under the same reflections ($31\bar{1}$, shown in Fig. 5b, and 400) as those for specimen I, and thus identified the Burgers vector, again, to be of the type ±a/2[011].

Thus, for the microstructures developed in specimen I and II, we found that two types of stacking faults were active in specimen I [a/3($1\bar{1}1$) and a/3($\bar{1}\bar{1}1$)], while for specimen II, there were no stacking faults observed. Dislocations were the most common defects in both specimens, and they were analyzed to have an inclined Burgers vector of the form a/2<011>. By checking the relative orientation of stacking faults and dislocations, it was shown that the Burgers vector was lying in the intersection of the paired active stacking faults.

The dramatic reduction of defect densities in specimen II can be understood by comparing the different processing procedures of the two specimens. The differentiation can be separated into two parts:

- the removal of the trench oxide by BHF etching, and
- annealing effects accompanying reoxidation.

The removal of oxide through BHF etching was unlikely to affect the defects directly, since the silicon is extremely insensitive to BHF etching. Therefore, reoxidation is believed to be responsible for the reduction of defect densities. In this work, the thermal reoxidation step was carried out at 1100°C for 40 min. This high annealing temperature should give atoms at imperfect sites (specimen I) enough energy to move back to their low energy perfect sites (e.g. by dislocation glide), thus reducing defect densities (specimen II.

Although the high temperature treatment may have annealed out defects produced during CVD growth, cooling from the high annealing temperature caused another problem in that the stresses induced by the differences of thermal expansion coefficients between Si and SiO_2 could introduce new defects into the epilayers.

Two further experiments were run to investigate this problem. Specimen III was first processed using the same procedures as described for specimen I (as-grown). This was followed by annealing in an N_2 ambient at 1100°C for 40 min to emulate the reoxidation anneal (used for specimen II), although with the original oxide intact. Specimen IV was processed as specimen I, but followed by removal of oxide and the same N_2 annealing condition, with the exception that the cavities were not reoxidized. (For TEM observation to protect the sidewall region during ion milling, polysilicon deposition at 600°C was used to fill up the cavity region; the low deposition temperature and match to Si in thermal expansion should have had a negligible effect on the microstructure.) The processing procedures for the four specimens are summarized in Table I.

Table I. Summary of Processing Procedures for Four Specimens

Specimen	Process General Description
I (as-grown)	1. Grown 0.3 μm of oxide. 2. Anisotropic RIE through oxide and 2.2 μm of Si. 3. Grow a conformal oxide at the sidewall and bottom. 4. RIE to open seed hole and expose Si. 5. Selective epitaxial growth by CVD. 6. Chemical-mechanical planarization to polish top surface. 7. Boron p^+ implant. 8. Contacts and metallization.
II	1. Same as specimen I (from step 1 to step 6). 2. BHF etching of oxide to form cavities. 3. Reoxidation of cavities (1100°C, 40 min). 4. Boron implant. 5. Contacts and metallization.
III	1. Same as specimen I. 2. Annealed in N_2 ambient at 1100°C for 40 min.
IV	1. Same as specimen I (from step 1 to step 6). 2. BHF etching of oxide to form cavities. 3. Annealed in N_2 ambient at 1100°C for 40 min. 4. LPCVD growth of polysilicon into cavities (for TEM preparation).

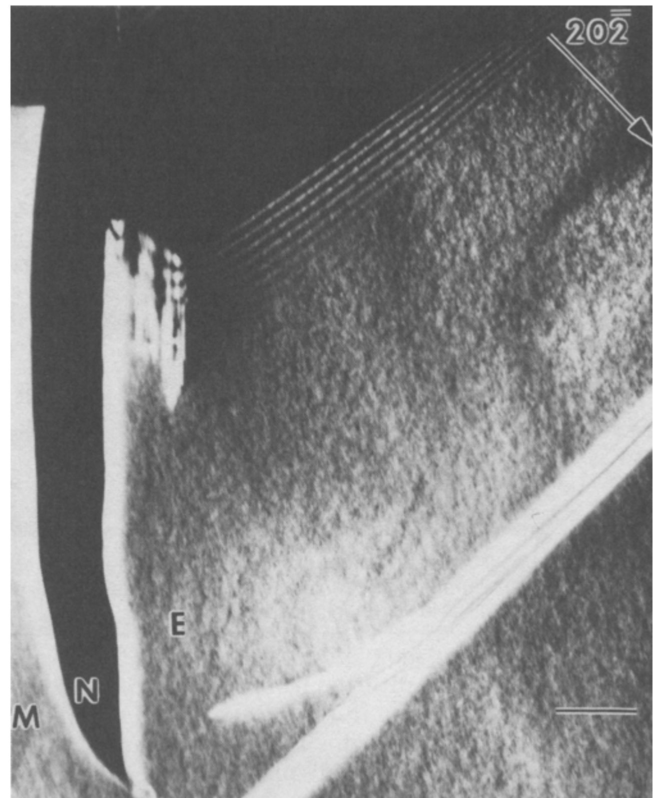


Fig. 6. Dark field image from a specimen III type sample. Defects were similar to those in the specimen I process; i.e. numerous dislocations, stacking faults, and twinned regions. The epitaxial SEG Si on the right (E), insulating oxide in the middle(N), and main substrate Si is on the left (M). The bar at lower right is 1/4 μm.

The microstructure of specimen III is shown in Fig. 6. Stacking faults were, again, major defects in the epilayer. One of them can be seen to have originated from the SEG sidewall interface and propagated at about 45° through the epilayer, ending at the SEG surface. The stacking fault was clearly bounded by two straight dislocations and produced fringes in between. The fringes were rendered out of contrast under the 202 reflection. The other defects appeared similar to those in the as-grown specimen (I), including dislocations and stacking faults. Comparison of the microstructures of specimens I and III showed that the defect densities were only slightly reduced by annealing alone.

For specimen IV (shown in Fig. 7), annealed without the oxide sidewalls, it was evident that most of these defects were eliminated. (The polysilicon cap layer, which was deposited after N_2 annealing, left a long, thin cavity due to incomplete deposition.) The defects observed in specimen IV were primarily dislocations; an array near the sidewall interface may be seen in Fig. 7. Unlike specimens I and III, stacking faults were rarely found in the epilayer of specimen IV.

The defects which existed in the SEG epilayer may result from several sources. It is evident that the existence of the amorphous oxide sidewall plays an important role in defect generation.[14] The silicon was initially grown from the seeded region; however, for the region next to the oxide, the bonding of atoms was disturbed, which may have generated imperfections in the crystal. These are referred to as growth mistake defects. The other source of defects may be generation by differences in the thermal expansion coefficients of silicon and SiO_2. The CVD growth of SEG, which was conducted at relatively high temperature, about 970°C for all four specimens, offers a source of thermal stress-induced defects at the sidewall interface during cool-down or later processing steps. These are referred to as thermal expansion defects.

The variation of microstructures in specimens III and IV may be related back to the respective processes. Specimens III and IV were annealed at the same thermal treatment conditions, but III was annealed with the presence of the oxide, while specimen IV was annealed without the presence of the oxide. High temperature treatment of the SEG material may be able to remove defects caused by growth mistakes and thermal expansion associated with CVD growth; however, new stresses will be generated in the oxide sidewall region due to heating/cooling for high temperature treatment. The new stresses could again generate new defects.

That specimen III exhibits a microstructure similar to the as-grown specimen suggests that a majority of defects may be due to thermal expansion mismatch effects. For specimen IV, high temperature annealing not only removed growth mistake defects, but also

thermal expansion defects. Because of the removal of the oxide before annealing, the thermal stresses due to the differences of thermal expansion coefficients could not be generated, and resulted in an improved microstructure, as expected. Longer annealing may possibly further reduce the residual dislocations in specimen IV. Similarly, specimen II contained visible defects only at the terminus of the oxide sidewall, where thermal expansion mismatch stresses would have been greatest.

Although the above process change markedly improved the SEG quality, it may not be a widely practical solution, since the passivating SiO_2 was removed from the wafers. However, it provides evidence about the nature of defect formation near the sidewall interface and suggests ways to minimize defect densities. It should be reiterated that the deep trench structure was a particularly severely stressed structure, with a long vertical oxide wall terminating sharply deep in the Si substrate. Specimen II, with reoxidized oxide cavities, exhibits a high quality SEG epilayer, and represents the probable best solution for fabrication of good devices. Annealing accompanied with reoxidation eliminated most of the preexisting defects caused by both growth mistakes and thermal expansion during CVD deposition, and only a low density of dislocations was introduced into the sidewall interface, as seen through TEM observations in this work. (Such defects might actually be beneficial, by reducing device interference.)

Generally speaking, high temperature treatment caused two opposite effects on material quality; that is, annealing out of pre-existing defects, and introduction of post-anneal defects generated through thermal stresses. The former effect depends on the energy of the original defects and crystalline growth kinetics, while the latter one relies upon the degree of thermal stresses generated, to induce defects. The competition of these two effects determines the quality of the grown reoxidized material. Further work should be concentrated on determining the detailed tradeoff between these two effects.

DIODE TESTS

Diodes were fabricated[9] from each of the first two processing techniques (specimen I and specimen II). Some of the electronic characteristics of these diodes are presented briefly in Table II, as an average from 20 devices located in different regions of the wafer. Diodes were not fabricated for specimen III and were not practical to fabricate for specimen IV. For specimen IA, the upper contact and p-type region were kept at least 5 μm (6 ±1μm) from the sidewall, the remainder of the SEG top surface being covered by oxide. For specimens IB and IIB, the upper p-type region was across the entire upper SEG face and intersected the sidewall. For all three, the other contact was made at the bottom of the wafer, directly below the SEG region. Thus, for IA, the current path did not notably intersect the defective region near the oxide wall, while for IB and IIB, the region near the wall contributed significantly to the diode behavior.

It can be seen that the defects in the sidewall region created significant problems in diode behavior. The SEG material was clearly of good quality, as illustrated by the near-unity ideality factor of the IA diodes. The ideality factor is significantly different from unity (1.78) for IB, and only slightly better (1.40) for the annealed and reoxidized specimen II. However, reverse leakage current simultaneously degraded slightly with the anneal and reoxidation (from 4.2 to 6.0 mA/cm²), so the degree of improvement was unclear. Reverse leakage current was not measured for specimen IA, but our values for similarly constructed devices have typically been ≤1μA/cm².

Since the defect content near the oxide sidewall in specimen II was still very high for electronic-grade material, it is not surprising that only a small improvement could be observed in diode behavior. We would expect, based on the idea that the oxide/Si thermal expansion difference was the root cause of the defects, that specimen IV would have shown the

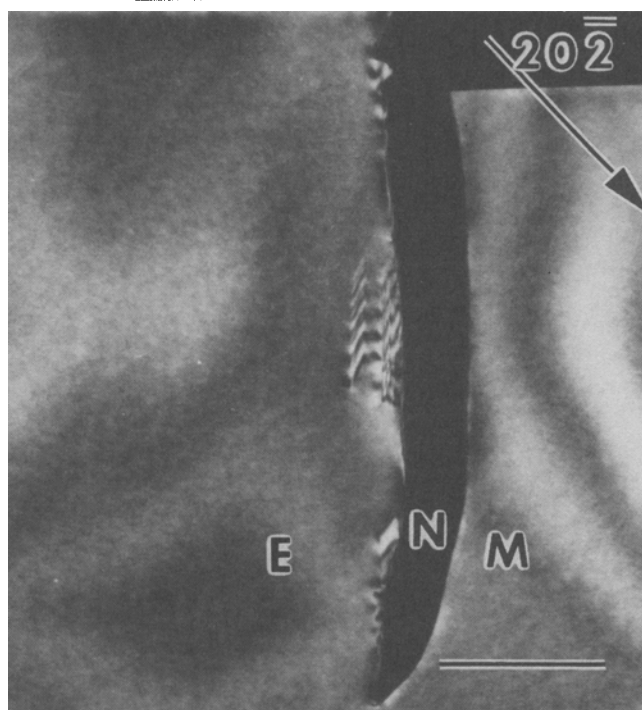


Fig. 7. Dark field imaging showing one of the few defective regions observed in specimen IV type materials. The stacking faults (and associated dislocations), when seen, were constrained to the region immediately adjacent to the sidewall and did not extend into the central SEG region. The main substrate Si is on the right (M), insulating oxide in the middle (N), and epitaxial SEG Si on the left (E). The bar at lower right is 1/2 μm.

Table II. Diode Performance

Specimen	Ideality (@0.45V)	Reverse Leakage (mA/cm²)
IA	1.01	—
IB	1.78	4.2
IIB	1.40	6.0

best characteristics. Unfortunately, it was not possible, within the scope of these experiments, to find a technique to fabricate diodes on those specimens in which they could be contacted on the entire SEG upper surface.

EXAMINATION OF CLSEG MATERIAL

Confined lateral selective epitaxial growth is one of the most promising techniques for obtaining large areas of thin SOI films. In CLSEG, the seed hole to the substrate has an enclosed cavity fabricated above it. The purpose of the enclosure is to restrict the epitaxial Si growth to the lateral direction, thus increasing the aspect ratio (breadth/width) of the overlayer Si. There were only a few publications which have mentioned this novel technique in device fabrication,[6,7,15] and the microstructural development in CLSEG growth has not been previously reported. In this section, we report the use of TEM to investigate the crystalline quality of CLSEG films.

Figure 8 shows a TEM micrograph of a typical CLSEG specimen. Perturbations of the top surface of the CLSEG film (which occurred above the seed window region) caused no apparent defects, and were due simply to the corresponding depth of the seed window during deposition of the sacrificial amorphous silicon used to delineate the cavity. The CLSEG film was measured to have a lateral/vertical aspect ratio of about 7.

It has been reported[7] that the crystal defect etching in 'tunnel epi' gave results which were quite similar to those seen in conventional ELO, including indications of dislocations, twins, and stacking faults. However, no defects were observed in the CLSEG specimens we examined. The contradiction may lie in that the seed window was patterned along ⟨110⟩ in the previously reported experiment,[7] while it was in a ⟨100⟩ direction in our CLSEG growths. The tendency for the ⟨110⟩ seed window orientation to give a poor quality epilayer has been described previously.[14,16]

Thermal expansion effects, also, did not seem to have had any appreciable effect. For the deep trench structure described above, the SEG region was firmly bounded by the whole wafer, and the oxide generated thermal stresses in the SEG layer and the substrate, resulting in many observable defects. In the CLSEG structure, however, the material was bounded at the bottom by the oxide/substrate and at the top by the upper oxide nitride layer which formed the cavity shell. The top oxide was about 0.07 μm thick, and the nitride was 0.20 μm. Unlike the deep trench specimens, the CLSEG film could be assumed to be tightly bounded at the bottom side, but nearly free to expand to the upward direction to relieve any thermal stresses. Also, less highly constrained corners were present. This may be the reason why a defect-free CLSEG region was observed.

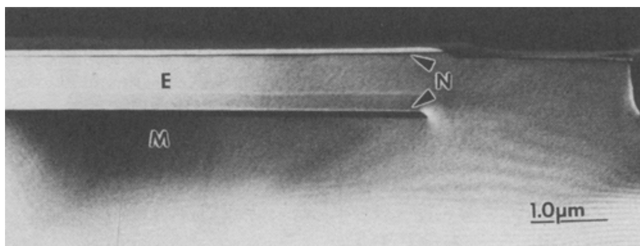


Fig. 8. Cross-sectional dark field image of a CLSEG (constrained lateral selective epitaxial growth) layer, and the adjacent region of substrate. The seed hole, at left, could be seen to be defect free, and the growth cavity was entirely filled. The epitaxial CLSEG material (E) is constrained above and below by insulating material (N).

In principle, any desired dimension of such SOI films could be grown successfully by adjusting the size of the sacrificial layer. However, oxide degradation is a potential problem in getting a large lateral dimension, because the reaction of silicon-containing gas and SiO_2 is more serious at longer deposition times. Thus, for a CLSEG cavity notably longer than those examined, the types of defects seen previously in other growths would probably begin to be introduced.

SUMMARY

The effects of oxide wall structures on the defect content of SEG Si have been investigated. It was found that substantial numbers of defects were located in the nearby SEG Si which had been grown over the walls at high temperature. These defects were observed in the TEM to be dislocations, stacking faults, and microtwins. Removal of the oxide followed by further high temperature annealing resulted in nearly complete removal of these defects.

We have concluded that while some of the initial defects may result from growth perturbations, many are caused by thermal mismatch induced stresses, resulting from differential thermal expansion of the oxide and Si. While removal of the oxide was not practical as a design modification for the devices fabricated here, redesign is possible in many cases to minimize the effects of thermal expansion mismatch.

One novel example of such a design, CLSEG, was also examined. Although not designed specifically for this purpose, the gross stress effects resulting from differential thermal expansion are notably reduced in this geometry. Possibly as a consequence of this, no structural defects were observed in the CLSEG materials examined.

ACKNOWLEDGMENT

We would like to thank Mr. John Denton and Mr. Darold Perry for their steady assistance. This work was partially supported by the Semiconductor Research Corporation under contract #93-55-108, and the National Science Foundation under grant No. DMR-9106308.

REFERENCES

1. S.M. Sze, *Semiconductor Devices–Physics and Technology,* (J. Wiley, 1985).
2. L. Jastrzebski, *J. Crystal Growth* 63, 493 (1983).
3. S.M. Sze, *VLSI Technology,* (McGraw-Hill, 1988).
4. S.W. Ruska, *Microelectronic Processing,* (McGraw-Hill, 1987).
5. A.S. Grove, *Physics and Technology of Semiconductor Devices,* (Wiley, 1967).

6. P.J. Schubert and G.W. Neudeck, *IEEE Elec. Dev. Lett.* 11, 181 (1990); P. Schubert and G.W. Neudeck, *Proc. of 8th Biennial Uni. / Govt. / Industry Microelectronics Symp.*, Westborough, MA, June 12–14, 1989.
7. A. Ogura and Y. Fujimoto, *Appl. Phys. Lett.* 55, 2205 (1989).
8. W.A.P. Claassen and J. Bloem, *J. Electrochem. Soc.* 127, 1836 (1980).
9. R. Bashir, Ph.D. (EE) Thesis, Purdue University (Dec. 1992).
10. J.A. Friedrich and G.W. Neudeck, *J. Appl. Phys.* 64, 3538 (1988).
11. C.H.J. Van Den Brekel, *J. Cryst. Growth* 23, 259 (1974).
12. D.R. Bradbury, T.I. Kamins and C.W. Tsao, *J. Appl. Phys.* 55, 519 (1984).
13. A. Ishitani, H. Kitajima, N. Endo and N. Kasai, *Jpn. J. Appl. Phys.* 1267 (1985).
14. C.I. Drowley, G.A. Reid and R. Hull, *Appl. Phys. Lett.* 52, 546 (1988).
15. P.J. Schubert and G.W. Neudeck, *IEEE Trans. Elec. Dev.* 37, 2336 (1990).
16. H. Kitajima, Y. Fujimoto, N. Kasai, A. Ishitani and N. Endo, *J. Cryst. Growth* 98, 264 (1989).