Dielectrophoresis and Chemically Mediated Directed Self-Assembly of Micrometer-Scale Three-Terminal Metal Oxide Semiconductor Field-Effect Transistors**

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Directed self-assembly techniques, such as fluidic self-assembly,[1–3] liquid-solder-based self-assembly,[4,5] self-assembly using capillary forces in fluid,[6,7] and shape-and-solder-directed self-assembly,[8,9] has been studied by many researchers in recent years in order to implement micro- and nanoscale electronic devices and to integrate heterogeneous materials and devices. These self-assembled systems can be used to construct hybrid devices with good electronic properties by using high-quality material to fabricate the initial device and then assembling these devices on other substrates. However, many challenges still remain. All studies to date have been demonstrated using devices or blocks containing devices that are 50 µm or larger. As the size of the devices is reduced, the efficiency and position precision is also reduced. We demonstrate here, for the first time, dielectrophoresis (DEP)[10] and chemically mediated fluidic self-assembly of individual three-terminal silicon metal oxide semiconductor field-effect transistors (MOSFETs) on a patterned substrate. Moreover, current–voltage (*I*–*V*) characteristics of the assembled MOSFETs were measured after the solution was evaporated and the contacts were annealed.

Single-crystal silicon MOSFETs of 2 µm width, 15 µm length, and 1.3 µm thickness with a polycrystalline silicon gate, silicon nitride spacers at the end of the gate stack, and gold source–drain contacts were designed and fabricated on a bond and etched back silicon-on-insulator (BESOI) wafer as shown in Figure 1a. (The fabrication of the MOSFET is described in the Experimental.) The MOSFETs were successfully released from the host BESOI wafer as described earlier.[11,12] Buffered hydrofluoric acid (BHF) was used to partially etch the buried oxide so that the oxide pillar held the device on the BESOI wafer. The wafer was transferred into deionized (DI) water with 0.05 % Tween 20, and the beaker was placed in an ultrasonic agitator. After the pillars were broken by ultrasonic agitation, the MOSFETs were released into solution, as shown in Figures 1b,c. Meanwhile, the assembly substrates (non-functionalized or functionalized with self-assembled monolayers (SAMs)) were formed on oxidized silicon wafers (which could be any substrate capable of sustaining low-temperature processes steps). A gold film (700 Å) with a chromium adhesion layer (300 Å) was deposited on the assembly substrate. Functionalized electrodes were formed using SAMs of 1,9-nonanedithiol ($HS(CH_2)_9SH$) by incubating the substrate in the solution for 24 h.

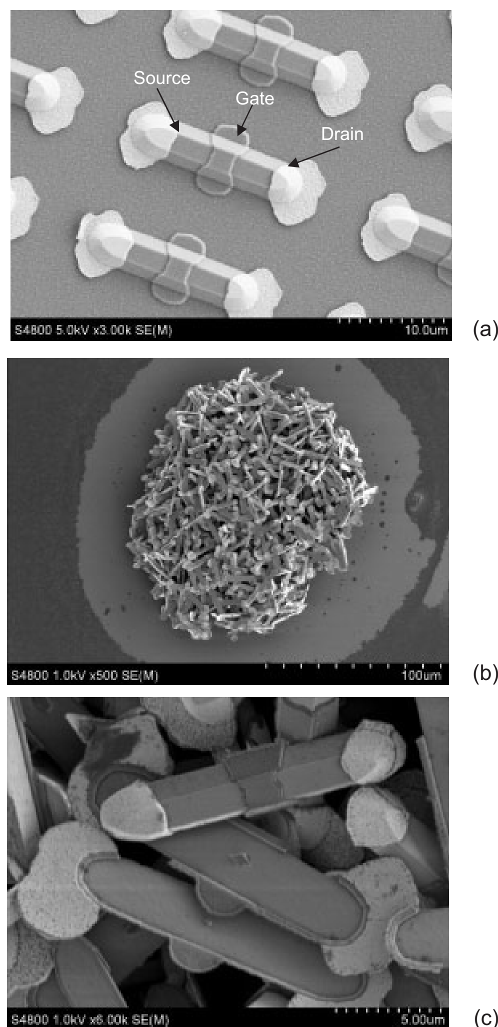

Figure 1. Field-emission scanning electron microscopy (FESEM) images of a) the completed silicon MOSFETs on a BESOI wafer, b) an aggregate of devices after drying, and c) close-up of the released device before assembly.

The process for DEP-mediated fluidic assembly, and the assembly in combination with 1,9-nonanedithiol using the

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released MOSFETs, are shown in Figures 2a–c and Figures 2d–f, respectively. The solution containing the three-dimensional (3D) MOSFETs is introduced onto a substrate. An alternating electric field is applied between two electrodes. As the MOSFETs settle onto the substrate, within an effective capture distance about equal to the distance between the electrodes,[13] and interact with the electric field, the devices experience a positive DEP force due to the metal contacts, and are assembled onto the binding positions, as shown in Figure 2b. In our earlier work,[11] we reported that an assembled resistor could be released from a binding position if the DEP force is turned off during the drying of the solution. To hold the assembled devices at the specific position, the following methods can be used: 1) the DEP force is still applied to the non-functionalized electrodes while the solution evaporates, as shown in Figure 2c; or 2) functionalized substrates are used so that the Au–S bonds between the device and the substrate hold the device in place during the evaporation of the solution, as shown in Figure 2f.

Using this strategy, experiments were performed as follows: 1) a 50 µl solution containing silicon MOSFETs was introduced onto a substrate with non-functionalized or functionalized metal electrodes. 2) An alternating current (AC) signal (5 V, 10 MHz) was applied using micromanipulator probes while a silicone rubber ring isolated the probes from the solution at the test sites. 3) The movement of the silicon MOSFETs were observed under a microscope and recorded using a digital camera. 4) The solution was completely dried while either the AC signal was still applied at the non-functionalized electrodes or the AC signal was applied into the functionalized electrodes for 1 h, allowing time to form Au–S bonds between the source/drain (S/D) contacts of the MOSFETs and the S/D electrodes of the functionalized electrodes; the signal was then turned off. Both procedures would hold the device at the original binding position. 5) Lastly, the substrates were annealed on a 250 °C hot plate for 25 min in order to reduce contact resistances between the gate, source, and drain contacts and the non-functionalized or functionalized electrodes.

In the S/D electrode structure shown in Figure 3a, the maximum electric-field gradient occurs near the edges of the S/D electrodes. Moreover, the permittivity of DI water and silicon is $80\varepsilon_0$ and $11.9\varepsilon_0$, respectively, where $\varepsilon_0 \sim 8.85\times10^{-12}$ F m^{-1}. The permittivity of metal can be treated as zero, while the conductivities of Au, Cr, and DI water are about 4×10^{7} S m^{-1}, 7×10^{6} S m^{-1}, and 2×10^{-4} S m^{-1}, respectively. The conductivities of an n-type polysilicon gate, n-type S/D regions, and a p-type MOSFET body are about 4.5×10^{3} S m^{-1}, 2.5×10^{4} S m^{-1}, and 5×10^{2} S m^{-1}, respectively. The calculated real part of the Clausius–Mossotti (CM) factor,[11] assuming silicon in DI water, is 1, while that of metal in DI water is also 1. Thus, the real part of the CM factor of the released MOSFETs is positive. The MOSFETs, when close to the S/D and gate region as shown in Figure 3a, would be expected to move between the S/D electrodes when an AC signal is applied to the electrodes. Since the real value of the CM factor is positive, the suspended devices move toward the maximum electric field gradient. As expected, when an AC signal with 5 V and 10 MHz was applied to the electrodes, the devices moved and were successfully assembled at the right binding positions, as shown in Figure 3b. The choice of frequency is semi-arbitrary, as long as the CM factor is maintained at a positive value. Subsequently, the drying process was performed while the AC signal was still applied to the electrodes. The assembled device stayed at the original binding position after the drying process was completed. Figure 3c is an optical microscopy image acquired after the solution was completely evaporated.

An experiment using functionalized electrodes was also performed. In this case, an AC signal with 15 V and 10 MHz was applied to the functionalized S/D electrodes for 1 h after a MOSFET was assembled in the correct binding position, in order to allow enough time to form Au–S bonds between the S/D contacts of the assembled MOSFET and the electrodes on the substrate. In this case, the voltage was increased to 15 V since the SAM layer can be thought of as an additional dielectric layer

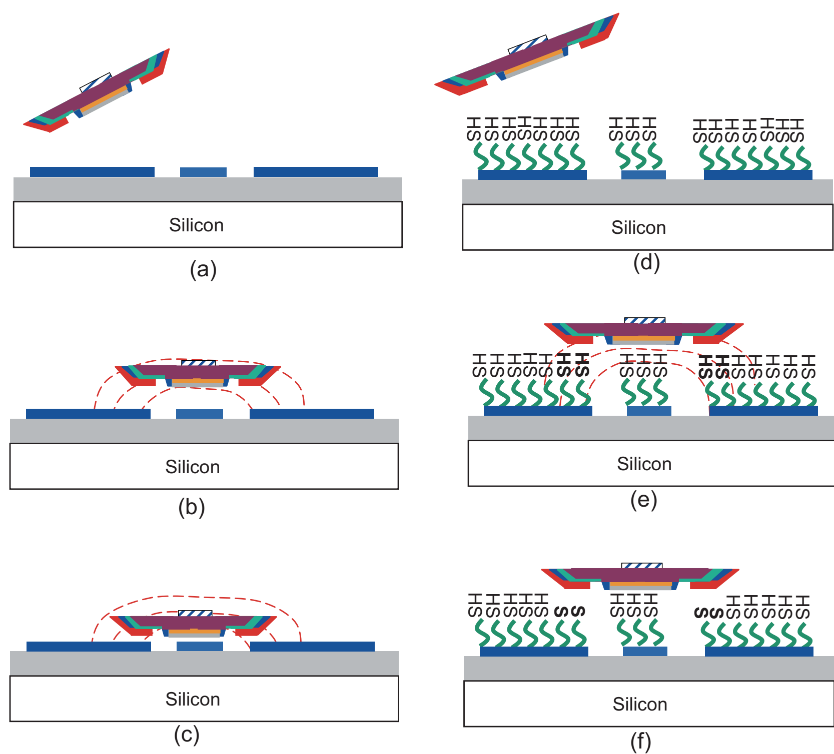

Figure 2. Schematic of a–c) DEP-mediated fluidic assembly, and d–f) DEP and chemically mediated fluidic assembly. Not to scale.

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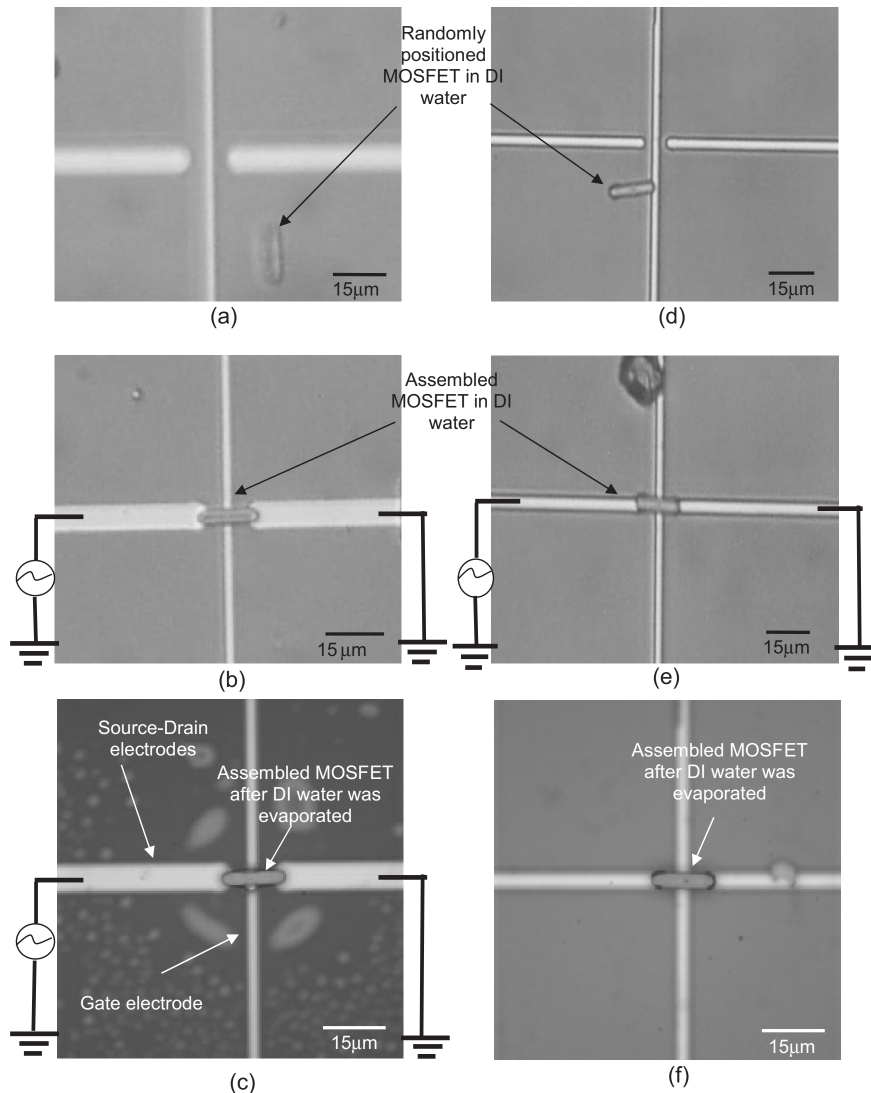

Figure 3. Non-functionalized electrode. a) Randomly distributed silicon MOSFET in DI water (0.05 % Tween 20) before alternating voltage is applied. b) Assembled silicon MOSFET in DI water after alternating voltage is applied. c) Assembled silicon MOSFET after DI water is completely dried, where the AC signal was on during the drying process. Functionalized electrode. d) Randomly distributed silicon MOSFET in DI water (0.05 % Tween-20) prior to application of AC signal. e) Assembled silicon MOSFET in DI water following application of AC signal. f) Assembled silicon MOSFET showing a good alignment after complete evaporation of the DI water, where the AC signal was off during the drying process.

at the interface. Then, the AC signal was turned off during the drying process. The assembled devices remained in the correct binding positions with good alignment, as shown in Figure 3f. After assembly, the devices were electrically characterized by measuring their transfer (source–drain current I_{ds} versus gate–source voltage V_{gs}) and output (I_{ds} versus drain–source voltage V_{ds}) characteristics before and after assembly, as shown in Figure 4. Clearly, the three terminal devices still show normal electrical characteristics after the assembly, demonstrating the success of this approach. There are some points to discuss. The current level was found to be reduced after the assembly by roughly one order of magnitude. It should also be noted that in the case using functionalized electrodes, the yield of assembly after the drying process was completed was approximately 30 %. Some devices were found to move slightly from the correct orientation, while others completely moved away from the binding site.

The average nearest-neighbor distance of the 1,9-nonanedithiol molecules within the SAM on the Au substrate is about 0.5 nm.[14] Assuming that the maximum number of Au–S bonds was formed on an area of 8 μm^2, this means that approximately 1.3×10^{10} Au–S bonds are formed in the S/D metal regions. The energy of the Au–S bond is estimated to be around 44 kcal mol^{-1}.[15] Therefore, the total binding energy due to Au–S bonding on a typical S/D metal region is 9.36×10^{-10} J. On the other hand, the surface tension of water on silicon dioxide is 42.7×10^{-3} N m^{-1}.[16] This corresponds to a surface energy per unit area of 42.7×10^{-3} J m^{-2}. Since the to-

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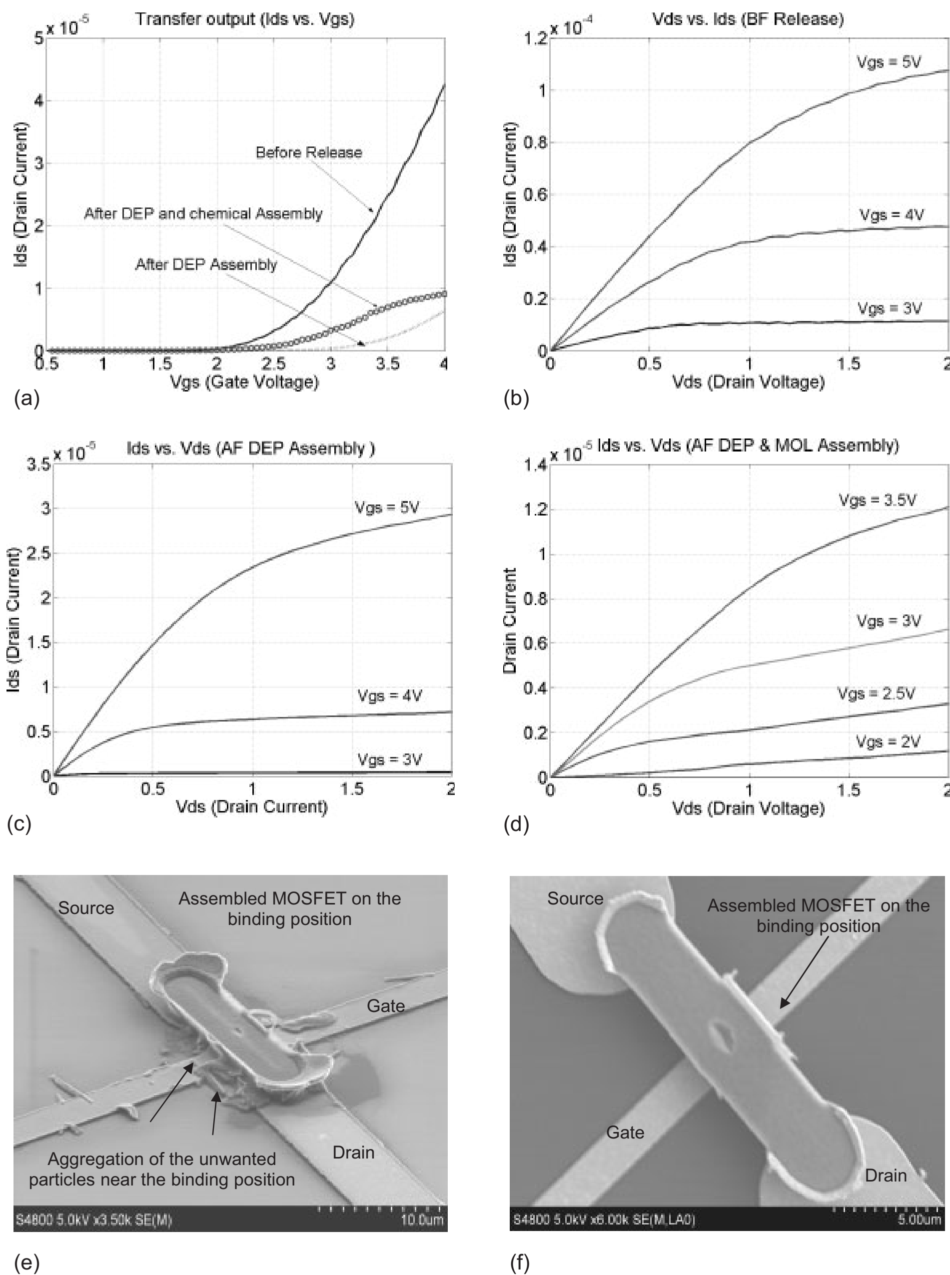

Figure 4. a) Transfer output of MOSFET before release, after DEP assembly, and after DEP and 1,9-nonanedithiol assembly at $V_{ds} = 1$ V. b–d) V_{ds} versus I_{ds} output of MOSFET as various gate voltages: MOSFET before the device was released (b), the assembled MOSFET using DEP (c), the assembled MOSFET using DEP and 1,9-nonanedithiol (d). FESEM images of e) the assembled device and unwanted particles on a binding position, and f) an assembled device.

tal area of the assembled MOSFET is 2 μm × 15 μm, the energy exerted on the assembled device during the evaporation process is around 1.3×10^{-12} J. This is less than the energy of the Au–S covalent bonds as calculated above. Therefore, the SAM layer can act as molecular glue to hold the devices in place. The fact that some devices moved slightly or completely away from the binding site during the evaporation period could be explained by defects in the SAM layer. The reduction of the current level after assembly can be explained by the presence of additional resistances (as explained in the Experimental) between the metal on the devices and the electrodes on the substrates. Additional factors to be further considered and optimized include: i) The solution needs to be free of unwanted metal contaminants and any other particulates. These can come from unwanted polycrystalline and metal fragments from the release process, and, when lodged between the devices and the substrate contacts, can be the source of defects and even cause parasitic leakage between

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the electrodes. Figure 4e shows metal particulates and contaminants close to the electrodes, while Figure 4f shows the assembled device without the presence of unwanted particles. ii) Leakage currents could flow through the back surface of the assembled silicon device since the device is exposed to air and not passivated. This can be easily overcome by deposition of a plasma-enhanced chemical vapor deposition (PECVD) oxide or nitride layer. iii) In a state-of-the-art, deep submicrometer MOSFET fabrication process, there is always a thin oxide layer between the silicon nitride spacer and the silicon as a stress relief layer. In our case, the silicon nitride spacer is in direct contact with the silicon surface due to the fact that the gate oxide needs to be protected during the release of the devices in BHF. The presence of silicon nitride on silicon could cause stress-induced leakage currents between the source and drain.

Some comments regarding the speed of the overall process are also in order. The current process of assembly consists of three stages: i) the device settling in the fluid and approaching the region of interaction in the DEP field, ii) assembly at the site using DEP and the SAM molecules, and iii) drying of the fluid before the electrical characteristics of the devices can be measured. The first stage takes less than 30 min and is a function of the volume of the fluid and size of the devices, while the second stage takes less than a few minutes if DEP alone is used, and about an hour if DEP and a SAM are used. The third stage is a function of the experimental setup and can be minimized depending on the amount of fluid used, the apparatus used to image the assembly process, and the means used to promote evaporation of the fluid. Since we used a cover glass to seal the fluid during the assembly for viewing and taking pictures, the evaporation was prolonged and was not optimized. In our setup this step took many hours, but we believe that this can be reduced to a more practical time (less than about an hour).

In addition, we observed that more than 80 % of the devices settled with the gate facing the substrate.[11,12] We believe that this could be due to the trapezoidal shape of the device, where the center of gravity causes the devices to tend to settle with the gate facing the substrate. If the devices were completely rectangular (i.e., bar shaped), we think that there would be more devices assembling in all directions. To address that scenario, we are pursuing a double-sided gate, which will allow the devices to land in either direction and still be able to function properly.

The process described in the paper can also be used to develop 3D integrated circuits on silicon wafers. A proposed approach to realize such 3D chips is shown in Figure 5, where SOI wafers are used to make the N-channel MOSFET (NMOS) and P-channel MOSFET (PMOS) devices, which are then released in fluid as described in this paper. The released MOSFETs can then be assembled on another substrate such that all NMOS devices are in one layer and all PMOS devices are in another layer. The process can be performed sequentially until the desired device is constructed. Metal layers to interconnect the device layers can then be interleaved between the assembly steps.

In conclusion, we designed and demonstrated a process for directed self-assembly of three-terminal single-crystal silicon MOSFETs using dielectrophoresis and chemical molecules. After the assembly, the devices are held in place during the drying process by either leaving the DEP voltage on or through the use of a SAM layer, although the latter was found to result in a lower efficiency. The devices were found to operate normally after the assembly; any reduction in current values can be explained by the presence of parasitic resis-

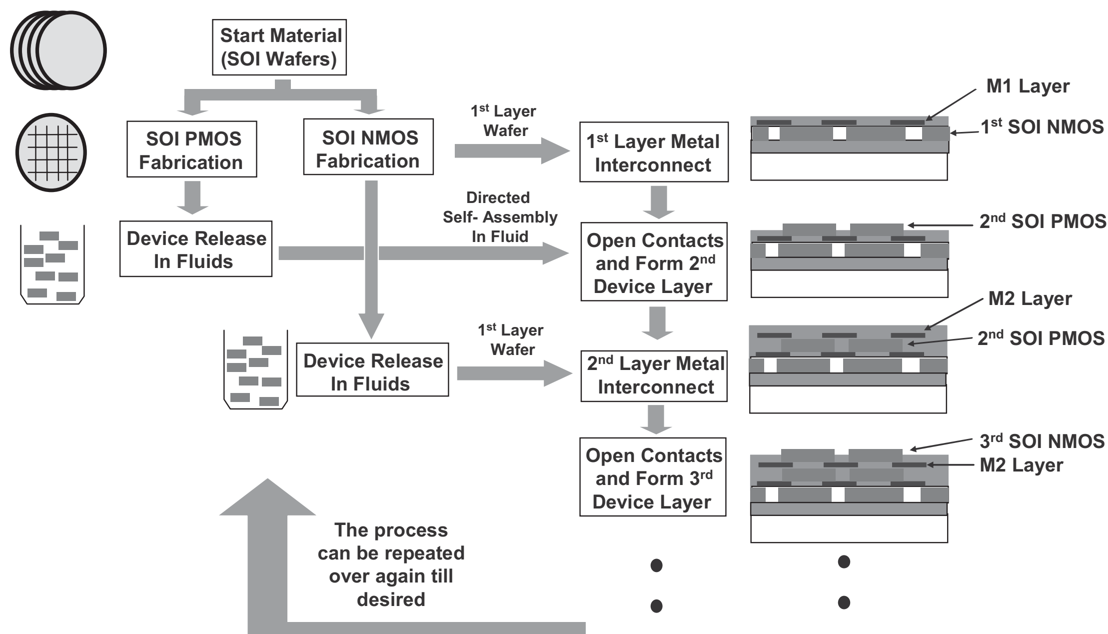

Figure 5. Proposed schematic process flow for the realization of three dimensional integrated circuits using directed fluidic self-assembly.

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tances between the device electrodes and the substrate electrodes. Hence, here we provide the foundation of a novel process for 3D integration of silicon devices and for heterogeneous integration of electronic, microelectromechanical system (MEMS), and other devices.

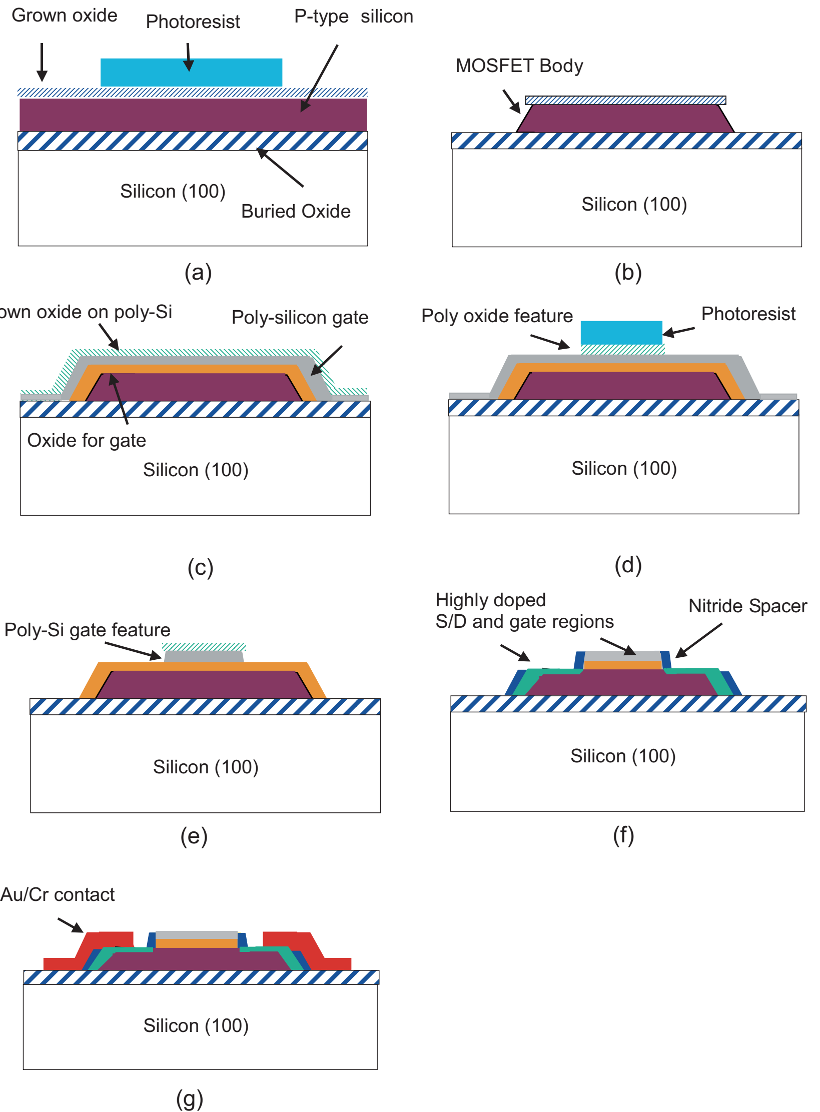

Figure 6. Process flow for the fabrication of the silicon MOSFETs.

Experimental

Fabrication Details for Constructing Silicon MOSFETs on a BESOI Wafer: The fabrication began with a commercially available BESOI wafer with a 1.3 μm top SOI layer and a 0.375 μm buried oxide layer, where the silicon layer was doped with boron and had a resistivity of 1–20 Ω cm. A 1600 Å thermal oxide was grown and 2 μm × 15 μm transistor-active areas were defined using a photolithography technique, as shown in Figure 6a. The oxide was etched using buffered hydrofluoric acid, resulting in oxide patterns for subsequent potassium hydroxide etching. The silicon layer was then etched at a temperature of 53 °C for 15 min in a solution consisting of 45 g KOH, 375 ml DI water, and 120 ml 2-propanol, as shown in Figure 6b. After removing the oxide mask, boron implants with doses of 5×10^{12} atoms cm^{-2} at 50 keV, 100 keV, and 150 keV were performed to achieve a MOSFET body doping concentration of $\sim2\times10^{17}$ atoms cm^{-3}. Subsequently, a 200 Å gate oxide was thermally grown, a 1500 Å gate polycrystalline silicon was deposited using a low-pressure chemical vapor deposition (LPCVD) system, and then a 200 Å poly oxide was grown thermally, as shown in Figure 6c. Photolithography and BHF etching were used to define the gate region features as shown in Figure 6d. These features were used as a mask for etching the polycrystalline silicon using KOH to form the gates, as shown in Figure 6e. This KOH etch step ensured that all stringers were removed from the sidewall of the MOSFET body. After removing the poly oxide mask, phosphorus implantation with a dose of 5×10^{14} atoms cm^{-2} and an energy of 25 keV was used to form the highly doped S/D and gate regions. The BESOI wafer was loaded into a LPCVD system after the native oxide on the S/D regions was completely removed, and then a 2000 Å silicon nitride was deposited. Since device release using BHF was performed, subsequent to the fabrication of the MOSFETs, the edge of the gate oxide needed to be protected using spacers formed by the silicon nitride layer. These spacers were formed by reactive ion etching (Drytek 384T) of the silicon nitride, as shown in Figure 6f. Lastly, a 700 Å thick chromium layer and a 1000 Å gold layer, which had the same thickness as that of the gate stack, were deposited sequentially in an electron-beam evaporator and patterned using a lift-off process, as shown in Figure 6g.

Extraction of Contact Resistances: Circuit models of the MOSFET before and after release are shown in Figures 7a,b, where R_d and R_s are the additional resistances formed at the interface between the metal on the MOSFET source and drain regions and the metal contact layers on the assembly substrate, and R_g is the resistance at the interface between the polycrystalline silicon gate on the MOSFET and the metal contact layer on the assembly substrate. We can use the linear region of the output characteristics (Fig. 4) to calculate the intrinsic channel resistance of the MOSFET using

$$R_{ch}^{int} = \frac{V_{ds}}{I_{ds}^{int}} \quad (1)$$

(where the superscripts "ext" and "int" correspond to values where external parasitic contact resistances are and are not taken into account, respectively) assuming the any other contact resistances are negligible for the case of the MOSFETs before release. The total resistance, including the external source–drain parasitic resistances, is given by

$$R_{total}^{ext} = \frac{V_{ds}}{I_{ds}^{ext}} = R_{total}^{ext} = R_s + R_d + R_{ch}^{int} \quad (2)$$

Using the charge-sheet approximation, the I–V characteristics of the MOSFET in the saturation region is given by

$$I_{dsat}^{int} = \mu_{eff} C_{ox} \frac{W}{L}\left((V_{GS} - V_t)V_{dsat} - \frac{m}{2}V_{dsat}^2\right) \quad (3)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, W and L are the gate width and length, respectively, m is the body effect, V_{dsat} is the drain voltage in the saturation region, V_{GS} is the gate voltage, and V_t is the threshold voltage. Similarly, the I–V equation of the

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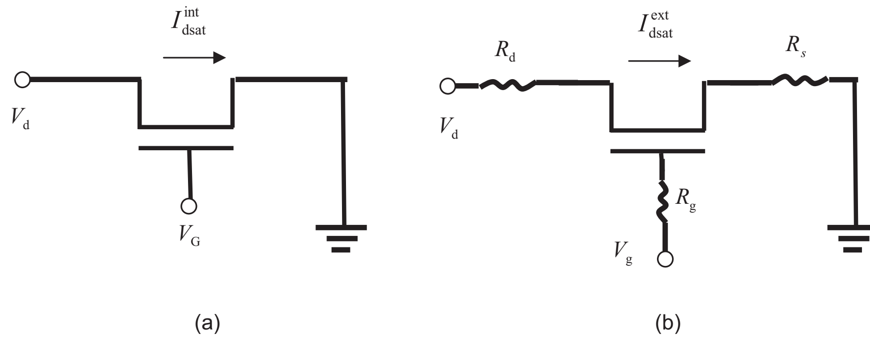

Figure 7. Circuit model of the transistor, a) without and b) with the parasitic contact resistances.

assembled MOSFET in the saturation region with the high contact resistance can be described by

$$I_{dsat}^{ext} = \mu_{eff} C_{ox} \frac{W}{L} \left((V_{gs} - V_t) V_{dsat} - \frac{m}{2} V_{dsat}^2 \right) \quad (4)$$

where V_{gs} is the gate voltage of the assembled MOSFET. Using the relationship

$$V_{gs} = V_{GS} + I_{dsat}^{ext} R_s \quad (5)$$

and substituting Equation 5 in Equation 4 and subtracting Equation 4 from 3, we obtain

$$\Delta I = \left| I_{dsat}^{ext} - I_{dsat}^{int} \right| = \mu_{eff} C_{ox} \frac{W}{L} I_{dsat}^{ext} R_s V_{dsat} \quad (6)$$

Then, $\Delta I / I_{dsat}^{int}$ can be calculated to be

$$\frac{\Delta I}{I_{dsat}^{ext}} = \frac{I_{dsat}^{int} R_s}{(V_{GS} - V_t) - \frac{m}{2} V_{dsat}} \quad (7)$$

Since the saturation region starts at

$$V_{ds} = V_{dsat} = \frac{(V_{GS} - V_t)}{m} \quad (8)$$

and the channel resistance is defined by

$$R_{ch}^{int} = \frac{V_{ds}}{I_{ds}^{int}} \quad (9)$$

Equation 7 can be rewritten as

$$\frac{\Delta I}{I_{dsat}^{ext}} = \frac{R_s}{\frac{m}{2} R_{ch}^{int}} \quad (10)$$

At $V_G = 4$ V and $V_{ds} = 50$ mV, the measured drain-to-source current, as shown in Figures 4b,c, are 2.8×10^{-6} A for the MOSFET before assembly and 9×10^{-7} A for the assembled MOSFET. Thus, $R_{ch}^{int} = 1.75 \times 10^4\ \Omega$ and $R_{total}^{ext} = 5.55 \times 10^4\ \Omega$. Using Equation 2 and these values, the calculated source–drain series contact resistances, $R_s + R_D$, is $3.8 \times 10^4\ \Omega$. In the saturation region, the average of the drain currents are 4.6×10^{-5} A and 6.8×10^{-6} A, respectively, at $V_G = 4$ V. Typically, the value of m falls between 1.1 and 1.4. Hence, the source-contact resistance calculated using Equation 10 is between $5.5 \times 10^4\ \Omega$ and $7 \times 10^4\ \Omega$. Both calculated resistances have the same order of magnitude. Therefore, the reduction of the current in assembled devices can be explained by parasitic source, drain, and gate contact resistances.

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