A Polysilicon Contacted Subcollector BJT for a Three-Dimensional BiCMOS Process

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***Abstract*—A novel polysilicon contacted subcollector (PCS) BJT was fabricated whose active device region was formed using selective epitaxial growth (SEG) of silicon. The fabrication of the PCS BJT is the first step in the development of a novel three-dimensional (3-D) BiCMOS process. To study the efficacy of the polysilicon collector contact, three types of BJT's were fabricated and their collector resistances were compared. These were the PCS BJT, a BJT fabricated in SEG silicon grown from a shallow trench incorporating a shallow collector contact with a buried layer, and a BJT fabricated in the silicon substrate with a shallow collector contact but no buried layer. The PCS BJT exhibited the smallest collector resistance in addition to showing excellent device characteristics, hence demonstrating the viability of the bipolar device for a 3-D BiCMOS process.**

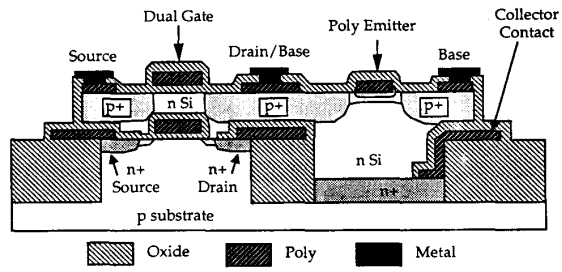

Fig. 1. Final cross section of the 3-D BiCMOS cell showing the 3-D CMOS inherently merged with the base of the BJT. Note the polysilicon contacted subcollector in the BJT.

I. Introduction

BiCMOS, a suitable merger of bipolar and CMOS, has received considerable attention in recent years for a variety of circuit applications, [1]–[3]. Simultaneously, there has been a trend to shrink device dimensions to obtain the maximum device performance. However, due to limitations in lithography and undesirable short-channel effects, the drive towards aggressive scaling of device dimensions has met with diminishing returns. Three-dimensional (3-D) integration provides a very viable solution to increase integration in the future. Applications of selective epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO) to obtain novel 3-D and other advanced devices have been previously reported [4]–[6].

To address the two above-mentioned issues, a 3-D BiCMOS process incorporating a 3-D CMOS inverter and a polysilicon contacted subcollector BJT (PCS BJT) was proposed earlier [7], [8]. The basic 3-D BiCMOS cell is schematically illustrated in Fig. 1. The novel 3-D BiCMOS fabrication process uses SEG/ELO of silicon for the 3-D integration and the inherent merging of devices. Note that the 3-D CMOS has its output inherently merged with the base of the bipolar transistor. One of the novel features of the BJT is its polysilicon contacted subcollector which helps reduce the active area and collector substrate capacitance. Owing to the fact that the bipolar is fabricated from a trench and its buried is contacted with the polysilicon layer, the trench depth and, hence, the BV_{ceo} can be tailored independently of the CMOS.

In this letter, we report the successful fabrication of the PCS BJT, which forms an integral part of the 3-D BiCMOS cell, and places more emphasize on the collector resistance and material quality issues. After the PCS BJT was fabricated, its collector resistance and other device parameters were measured and compared with BJT's incorporating a shallow n^+ collector contact. Simulations reported earlier showed that the collector resistance of the PCS BJT is comparable to that of a conventional BJT with a deep n^+ collector plug [7], [8]. In addition to showing the viability of the 3-D BiCMOS process, the PCS BJT is also a good candidate for a new bipolar technology providing minimum collector–substrate capacitance and the flexibility of speed and/or power applications on the same chip.

II. Fabrication

The fabrication process started with n-type, 1–5-$\Omega \cdot$ cm, {100} silicon wafers. Device structure patterns were oriented along the ⟨100⟩ direction on the {100} plane to reduce growth defects and enhance the SEG material quality. After growing a field oxide, RIE using Freon 115 was used to anisotropically etch through the oxide and 1 μm of silicon substrate. A conformal thermal oxide layer

Manuscript received March 20, 1992; revised May 10, 1992. This work was supported by the Semiconductor Research Corporation under Contract 92-SJ-108.

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IEEE Log Number 9202160.

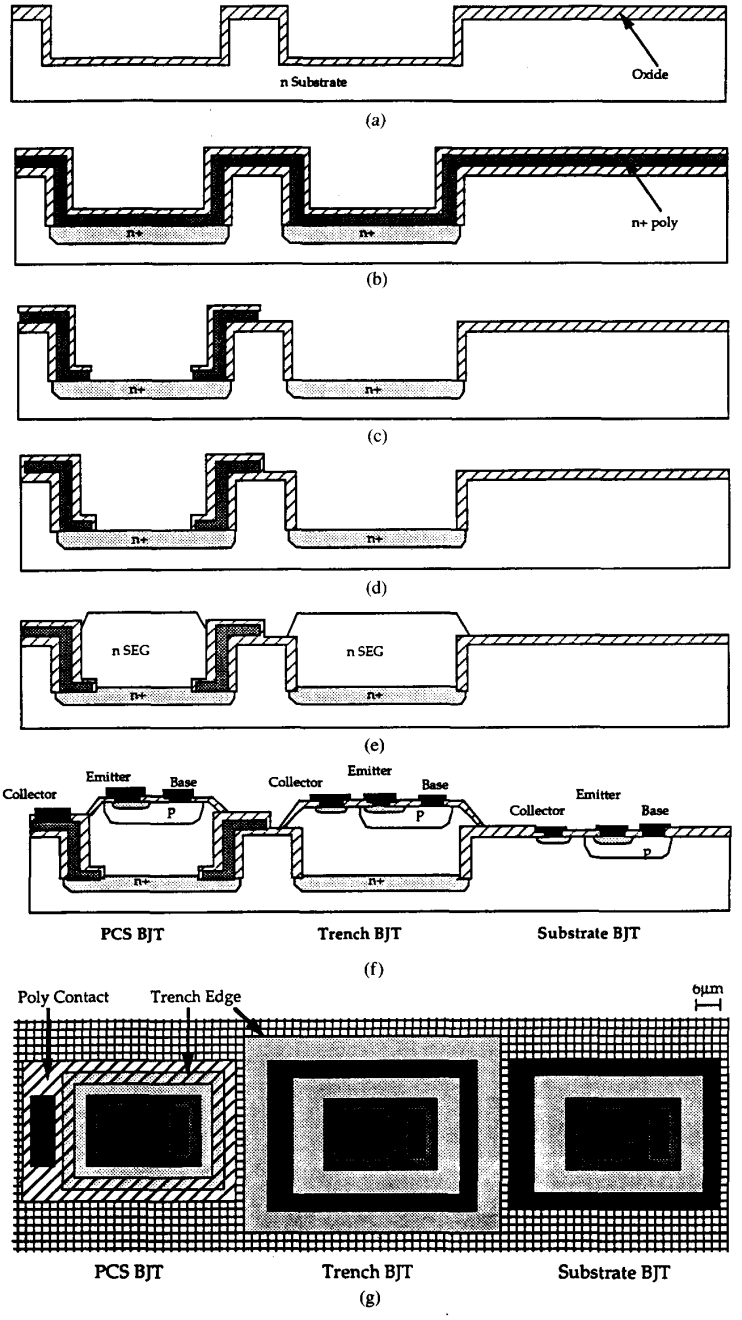

Fig. 2. (a)–(f) Fabrication process of the three types of BJT's fabricated in this study. (g) Layout of the three types of BJT's with 12-μm × 10-μm emitter.

was then formed on the sidewall and bottom of the trench. Next, anisotropic RIE was used again to etch out the oxide only in the bottom of the trench, hence exposing the silicon. Following surface cleaning, 0.5 μm of amorphous silicon layer was deposited and doped with phosphorus using a $POCl_3$ source at 950°C for 15 min. The wafers were then oxidized to form 0.3 μm of poly-oxide. The oxidation was also used to drive in the phosphorus through the polysilicon and into the substrate to form a buried layer. The polysilicon contact was then defined by etching the poly-oxide and polysilicon using a photoresist mask. All of the oxide and polysilicon was removed from the trench BJT regions while the contacts were defined in the PCS BJT's. Next, 0.12-μm oxide was formed on the

TABLE I
SUMMARY OF MEASURED PARAMETERS FOR THE THREE TYPES OF BJT'S

Measured Parameter \ Device Type	Emitter Size (μm^2)	Substrate BJT	Trench BJT	PCS BJT
Collector Resistance R_c (Ω)	36 × 36	190.4	63.3	35.9
	24 × 24	191.9	73.1	44.4
	12 × 12	202.7	95.0	65.5
Collector–Base Leakage J_{CBO} (A/cm^2)	36 × 36	1.4×10^{-6}	2.3×10^{-6}	12.1×10^{-6}
Ideality Factor η	C–B/36 × 36	1.01	1.06	1.4
	E–B/36 × 36	1.01	1.04	1.1
Collector–Emitter Breakdown BV_{CEO} (V)	36 × 36	57.4	12.3	12.7
β	36 × 36	50	50	50

exposed silicon and the sidewall of the polysilicon contact. A maskless anisotropic RIE was then used again to etch the oxide from the silicon substrate and open the seed-hole for SEG/ELO. The wafers were annealed at 900°C for 20 min in dry N_2 to remove RIE damage.

The SEG/ELO of silicon was performed next, in a standard reduced-pressure pancake-type RF-heated epitaxial reactor. A 5-min hydrogen bake and 30 HCl etch, both at 970°C, were used prior to growth. SEG/ELO was then grown from the silicon seed holes at 970°C, and 40 torr at a growth rate of 0.12 μm/min to result in 4.5 μm of growth. The SEG was n-type with a doping of about 8×10^{15} cm^{-3}. After the SEG, boron was implanted in the devices for base formation at an energy of 40 keV and a dose of 6×10^{13} cm^{-2}. The base was driven in by growing a wet oxide for 15 min at 1000°C. The emitter was then implanted at an energy of 25 keV and a dose of 5×10^{15} cm^{-2}. The emitter was activated by a wet oxidation for 15 min at 1000°C. Contacts were opened and approximately 0.25 μm of Al–1% silicon alloy was sputter deposited and defined using lift-off on the three types of devices. The wafers were finally annealed at 415°C in dry N_2 for 20 min. The cross section of the three types of BJT's at different steps is shown in Fig. 2(a)–(f). Fig. 2(g) shows the layout for 12-μm × 12-μm emitter devices.

III. EXPERIMENTAL RESULTS / DISCUSSION

The PCS BJT fabricated herein was designed to be non-self-aligned, yet it maintained all the novel features of the BiCMOS BJT. All three types of BJT's were fabricated on the same die and designed to have identical profiles and geometries. The three types of BJT's showed typical I_c versus V_{ce} curves. Fig. 3 shows the output characteristics of a typical PCS BJT. Table I lists some of the measured electrical parameters for the three types of devices which were averaged over 20 devices. The trench BJT's have a lower collector resistance than the substrate BJT's due to the presence of the buried layer formed by the diffusion of phosphorus from the polysilicon into the substrate at the bottom of the trench. The PCS BJT's have the least collector resistance because of the fact that

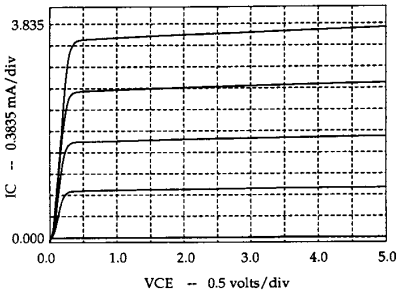

Fig. 3. Common emitter dc I–V characteristics of a typical PCS BJT. The base current step is 20 μA and the final base current is 80 μA.

they have a buried layer and their collector is contacted by the doped polysilicon layer, not by a shallow emitter contact. The polysilicon sheet resistivity was measured by four-contact resistors to be 10.2 Ω/sq. The collector–emitter breakdown voltage BV_{ceo} for the PCS BJT's was approximately 12 V. It is important to note that this value of BV_{ceo} could be changed by changing the trench depth. The collector–base diode reverse leakage currents were also measured at -3 V to examine the material quality. As expected, the substrate devices exhibited the smallest leakage while the PCS BJT had the highest. The slight increase in the leakage current in the trench BJT's over the substrate BJT's could be attributed to the fact that the SEG/ELO was grown out of a surface which was exposed to RIE damage four times prior to the selective growth, and the damage might not be removed completely in the subsequent oxidations and anneals. The increase of almost an order of magnitude in the leakage current in the PCS BJT over the trench BJT's could be attributed to the difference in the two structures. These differences include SEG/ELO growth over the poly-contact step and the growth along a rough poly-oxide surface in the PCS BJT. Preliminary work has shown that the use of arsenic as a dopant from implant or from spin-on-dopant diffusion results in a smoother poly surface. Work is currently underway to fabricate transistors with arsenic as the

dopant for the polysilicon contact. The SEG/ELO could be planarized using a chemical-mechanical polishing scheme which would make the top surface planar and remove facets and end effects [5], [6].

IV. Conclusions

The purpose of this letter was to report the results of the fabrication of a novel polysilicon contacted subcollector (PCS) BJT which would be used in a 3-D BiCMOS process. The polysilicon used to make the collector contact was doped with phosphorus using gaseous phase doping. The PCS BJT exhibited the smallest collector resistance when compared to a substrate BJT and a trench SEG BJT, exhibited excellent device characteristics, and hence demonstrated the viability of its use in a 3-D BiCMOS process.

Acknowledgment

The authors would like to thank J. Siekkinen, J. Glenn, and M. Young for ion implantation and mask generation, and P. Gilbert, and C. Subramanian for helpful discussions.

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