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Monolayer MoS_2 Nanoribbon Transistors Fabricated by Scanning Probe Lithography

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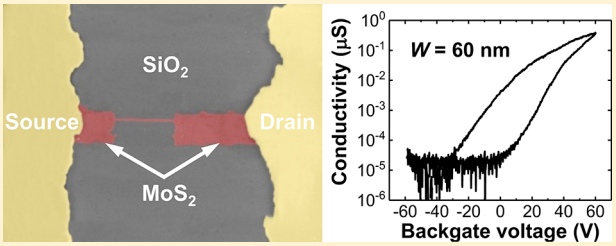
Supporting Information

ABSTRACT: Monolayer MoS_2 is a promising material for nanoelectronics; however, the lack of nanofabrication tools and processes has made it very challenging to realize nanometer-scale electronic devices from monolayer MoS_2. Here, we demonstrate the fabrication of monolayer MoS_2 nanoribbon field-effect transistors as narrow as 30 nm using scanning probe lithography (SPL). The SPL process uses a heated nanometer-scale tip to deposit narrow nanoribbon polymer structures onto monolayer MoS_2. The polymer serves as an etch mask during a XeF_2 vapor etch, which defines the channel of a field-effect transistor (FET). We fabricated seven devices with a channel width ranging from 30 to 370 nm, and the fabrication process was carefully studied by electronic measurements made at each process step. The nanoribbon devices have a current on/off ratio > 10^4 and an extrinsic field-effect mobility up to 8.53 $cm^2/(V\ s)$. By comparing a 30 nm wide device with a 60 nm wide device that was fabricated on the same MoS_2 flake, we found the narrower device had a smaller mobility, a lower on/off ratio, and a larger subthreshold swing. To our knowledge, this is the first published work that describes a working transistor device from monolayer MoS_2 with a channel width smaller than 100 nm.



KEYWORDS: *MoS_2 transistor, monolayer, narrow channel, scanning probe lithography*

MoS_2, a widely studied transition metal dichalcogenide semiconductor, is potentially well suited for electronic applications, due to its large band gap (1.9 eV for monolayers), acceptable mobility, and two-dimensional atomic layer structure that allows for a high degree of electrostatic control over its electrical conductivity.[1,2] Field-effect transistors from monolayer MoS_2 can achieve a current on/off ratio larger than 10^8, room-temperature carrier mobility of ∼150 $cm^2/(V\ s)$, and near-thermionic subthreshold swing, making monolayer MoS_2 a promising candidate for low-power electronics.[1,3−6] Because of these intriguing electronic characteristics, there has been significant research into electronic devices made from MoS_2; however, the field is still immature and considerable challenges remain, especially for the realization of nanometer-scale devices.

Nanometer-scale MoS_2 transistors are desired for a high device density and low-power operation;[3,7,8] however, there are only a few published articles that describe the fabrication of these devices, owing to the difficulty of device fabrication. For example, multilayer MoS_2 with a thickness of 5−15 nm (7−25 layers) was formed into nanoribbons as narrow as 40−65 nm using electron beam lithography (EBL).[9−11] Transistors based on these multilayer ribbons had current on/off ratios of 10^5 to 10^7 and a room-temperature mobility of 1.25−31 $cm^2/(V\ s)$. In one study, a monolayer MoS_2 transistor with a channel width of 200 nm was fabricated using oxidation scanning probe lithography.[12] The monolayer transistor had a current on/off ratio of 200 and room-temperature mobility of 0.12 $cm^2/(V\ s)$. Smaller structures have been demonstrated in monolayer MoS_2, for example, 20 nm structures fabricated using EBL,[13] and 10 nm structures fabricated using helium ion beam milling.[14] These structures were, however, not integrated into working transistors. To our knowledge, there has been no published article that describes a working transistor device from monolayer MoS_2 with a channel width smaller than 100 nm.

A key technical challenge for the fabrication of monolayer MoS_2 transistors is the compatibility of the materials and the materials processing. For example, even low electron doses used in EBL can induce defects such as sulfur vacancies in monolayer MoS_2,[15,16] which has a more sensitive surface than multilayer MoS_2 due to a higher surface to volume ratio.[17] Ion beam lithography can also damage sensitive electronic materials.[18,19] As an alternative to these processes, we propose SPL, which avoids the exposure of device materials to radiation.[20] SPL has been shown to overcome materials and process compatibility issues and fabricate nanoelectronic

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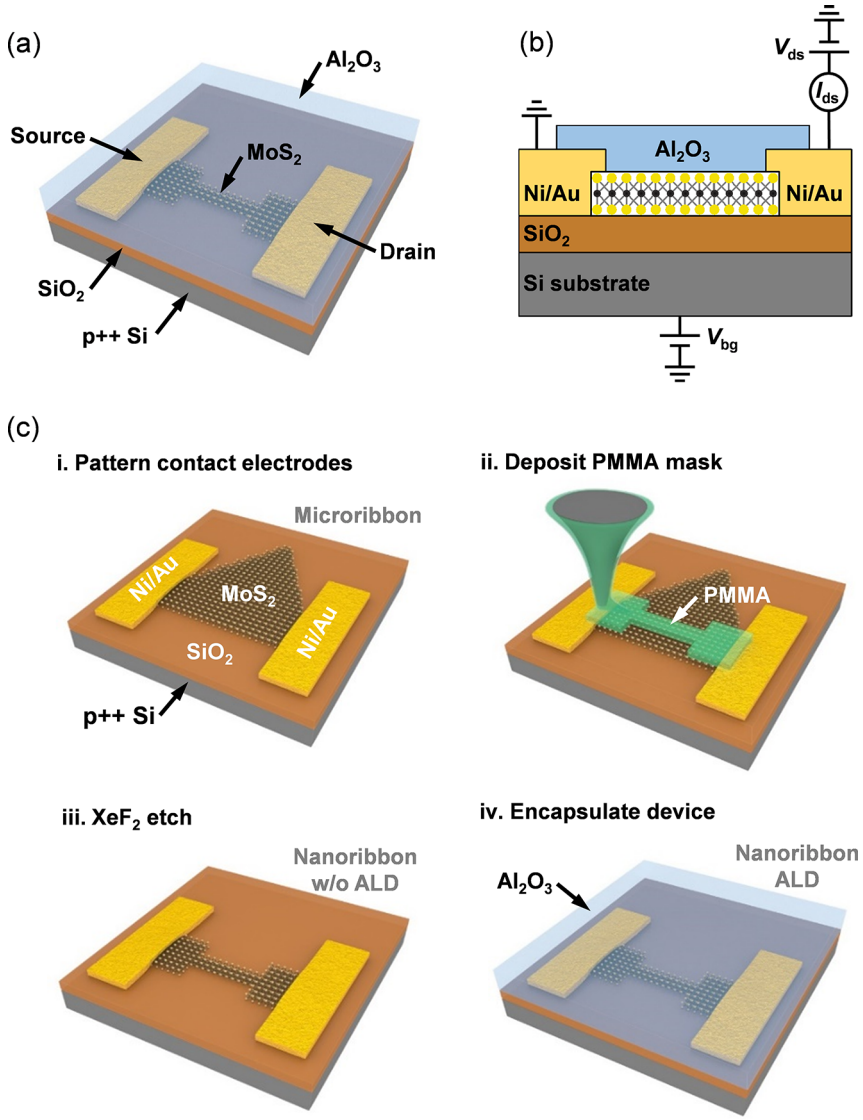

Figure 1. (a) Schematic of the monolayer MoS_2 nanoribbon FET. (b) Cross-sectional view of the FET, along with the electrical connections used to characterize the device. (c) Process flow for device fabrication.

devices such as silicon nanowire transistors,[21,22] graphene devices,[23−27] and WSe_2 transistors.[28]

This article reports the fabrication of monolayer MoS_2 nanoribbon FETs as narrow as 30 nm, realized using SPL. An atomic force microscope (AFM) tip deposited a nanometer-scale constricted polymer on a prefabricated microribbon FET as an etch mask and XeF_2 etched unmasked MoS_2, forming a nanoribbon FET. One 30 nm wide monolayer FET achieved a mobility of 8.53 $cm^2/(V\ s)$ and an on/off ratio of 2×10^5, on par with multilayer MoS_2 nanoribbon FETs reported to date. We found the electrical properties of MoS_2 FET degrade after nanoribbon formation, while atomic layer deposition (ALD) of high-κ dielectric on nanoribbon devices improves the mobility and on/off ratio. Finally, we observed an increase in threshold voltage after nanoribbon formation and a decrease in threshold voltage after ALD passivation.

Figure 1 shows the device design and fabrication process flow. Figure 1a,b shows the top and side views of the monolayer MoS_2 nanoribbon FET and its components and electrical connections. The device consists of a narrow monolayer MoS_2 channel, electrical contacts for the source and drain consisting of 30 nm gold on 5 nm nickel, a 285 nm SiO_2 gate dielectric, and a degenerately p-doped silicon back gate. A layer of 10 nm Al_2O_3 provides passivation. Figure 1c illustrates the device fabrication process flow. The fabrication started with the growth of monolayer MoS_2 by chemical vapor deposition[29] on a SiO_2/Si substrate (i). Atomic force microscopy and Raman spectroscopy confirmed that the MoS_2 is a monolayer (see Supporting Information). Contact electrodes were defined using optical lithography, forming a single-layer MoS_2 microribbon device. We fabricated seven devices with various feature sizes. The channel width varied over the range 6.9−37.5 μm, and the channel length varied over the range 3.9−6.9 μm.

We used thermal dip-pen nanolithography (tDPN) to form constrictions in the microribbons (ii).[23,30] In tDPN, a heated AFM tip writes a solid ink onto a substrate and the temperature gradient between the tip and the substrate controls the ink flow. In this process, a diamond-coated AFM cantilever tip[31] deposited a narrow ribbon of poly(methyl methacrylate) (PMMA) (M_w = 542 900) across the electrodes. The deposited polymer serves as an etch mask in

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subsequent steps. We were able to tailor the width of the deposited lines by controlling polymer mask deposition from the heated AFM tip,[32] with a lower tip temperature and higher tip speed, producing narrower ribbons. The tip temperature ranged from 210 to 300 °C, and the tip speed ranged from 100 to 1000 nm/s. To protect the MoS_2-metal contact during etching, the tip also deposited larger regions of PMMA near both contacts. (See the Supporting Information for additional details.) Next, we used XeF_2 gas to etch the unmasked MoS_2, forming a MoS_2 nanoribbon device (iii).[33] We choose XeF_2 vapor over plasma etching because XeF_2 has a higher selectivity of MoS_2 to PMMA. Raman spectroscopy on tip-defined MoS_2 microribbon channels of nanoribbon devices confirmed that the tDPN process does not damage the MoS_2 (see Supporting Information).[16] Finally, on some transistors, we used atomic layer deposition to encapsulate the nanoribbon device with 10 nm Al_2O_3 (iv). The ALD passivation layer was introduced with the goal of improving carrier mobility[34] and slowing degradation[35] by protecting the devices from air and water vapor. Table 1 summarizes the dimensions and electronic

Table 1. Summary of Monolayer MoS_2 Nanoribbon FETs[a]

device	W (nm)	L (μm)	μ (cm^2/(V s))	I_{on}/I_{off}	SS (V/dec)
A	30	0.16	8.53	2×10^5	8.2
B	36	1.93	1.05	1×10^3	12.8
C	60	2.95	4.33	4×10^4	10.1
D	154	1.42	0.36	2×10^3	6.0
E	230	3.75	1.71	2×10^4	6.4
F	270	1.26	4.18	1×10^6	5.6
G	370	2.10	1.19	1×10^5	5.1

[a]Devices A–C were passivated with 10 nm ALD Al_2O_3, while Devices D–G were unpassivated.

characteristics of seven monolayer MoS_2 nanoribbon transistors fabricated using this process, with a width ranging from 30 to 370 nm. Devices A–C were passivated with 10 nm ALD Al_2O_3, while Devices D–G were unpassivated.

Figure 2 shows an example MoS_2 monolayer nanoribbon device, Device B from Table 1. Figure 2a shows the false-colored scanning electron microscopy (SEM) image of the device, and Figure 2b shows the magnified SEM image. The images exhibit a 36 nm wide and 1.93 μm long nanoribbon in series with two microribbon segments, showing that our SPL technique is capable of fabricating continuous MoS_2 nanoribbons of an L/W aspect ratio of 54.

Figure 3 shows the transfer and output characteristics of a monolayer MoS_2 FET (Device C in Table 1) that was measured at each stage of fabrication, as a microribbon, after patterning down to a nanoribbon with tDPN, and after coating with an ALD passivation layer. The microribbon and nanoribbon have very different aspect ratios (L/W = 0.48 for the microribbon and 49 for the nanoribbon), and the nanoribbon is in series with two microribbon segments. To normalize the measurements, the effective conductivity per square is calculated as $\sigma_{\blacksquare} = I_{ds}/V_{ds}\Sigma(L/W)$, where $\Sigma(L/W)$ is the sum of L/W over all of the channel segments in series. Figure 3a shows the transfer curves of the microribbon (black) and the nanoribbon before (red) and after ALD passivation (blue). Three important metrics of a field-effect transistor were extracted from the transfer curves: extrinsic field-effect mobility $\mu = d\sigma_{\blacksquare}/C_g dV_{bg}$, current on/off ratio I_{on}/I_{off}, and subthreshold swing SS. The mobility is calculated using the gate dielectric

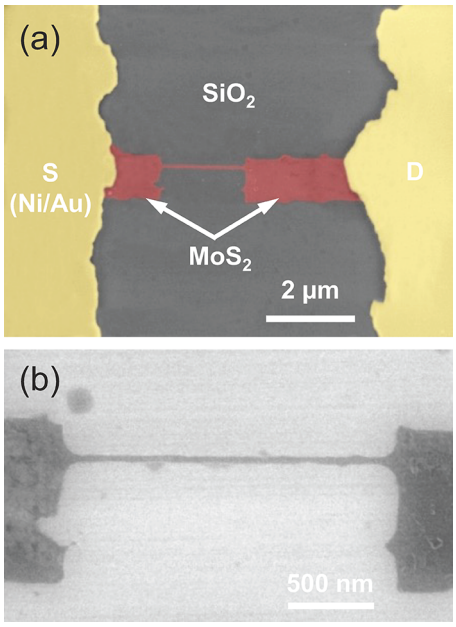

Figure 2. (a) False-colored SEM image of a 36 nm wide monolayer MoS_2 nanoribbon device (Device B). (b) Magnified SEM image of the MoS_2 nanoribbon device shown in part a.

capacitance per unit area of 285 nm thick SiO_2 (C_g = 12.1 nF/cm^2).

The microribbon transistor in Figure 3 is 11.6 μm wide and 5.6 μm long, with a mobility of 25.54 cm^2/(V s), a current on/off ratio of 1×10^6, and a subthreshold swing of 2.3 V/dec. These values are typical of monolayer microribbon transistors on SiO_2/Si substrates.[36−39] After nanoribbon formation, the device had a nanoribbon that is 60 nm wide and 2.95 μm long, and the electronic properties changed to a mobility of 0.97 cm^2/(V s), a current on/off ratio of 5×10^3, and a subthreshold swing of 6.4 V/dec. Several factors could affect the observed reduction in mobility and on/off ratio after nanoribbon formation, such as an increased edge disorder from etching, a more prominent role of edge roughness and defects in nanoribbons, or an increased surface scattering due to the presence of PMMA residue. The increased subthreshold swing likely resulted from an increased interface trap density.

After ALD passivation, the nanoribbon device had a mobility of 4.33 cm^2/(V s), a current on/off ratio of 4×10^4, and a subthreshold swing of 10.1 V/dec. The increase in mobility and current on/off can be attributed to a charged impurity screening by the high-k dielectric passivation. An increase in subthreshold swing likely resulted from a higher interface trap density. The ALD process could have introduced additional interface traps due to the presence of H_2O in the reaction.[40] The transfer curves of the nanoribbon device are noisy compared with that of the microribbon device. The increased noise after nanoribbon formation is a result of contributions from (1) larger carrier number fluctuations in the channel due to an increased density of interface traps, which capture and release carriers,[6] and (2) mobility fluctuation in the narrow channel.[41] Finally, the hysteresis in the nanoribbon device is significantly larger than that in the microribbon device, which can be explained by an increased density of defects and traps in nanoribbons.[42]

Figure 3b–d shows the output characteristics of the microribbon device and the nanoribbon device before and

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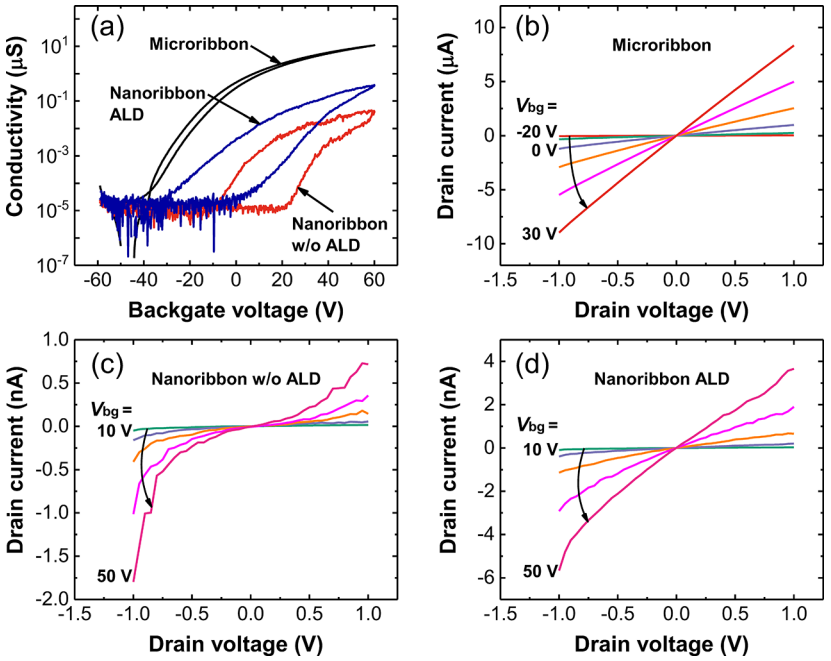

Figure 3. Electrical performance of a monolayer MoS_2 FET (Device C). (a) Transfer curves of the microribbon device and the nanoribbon device before and after ALD passivation. V_{ds} = 0.5 V. (b) Output curves of the microribbon device. (c) Output curves of the nanoribbon device before ALD passivation. (d) Output curves of the nanoribbon device after ALD passivation. V_{bg} was swept with a 10 V step in parts b–d.

after ALD passivation. Figure 3b shows a linear dependence of drain current on drain-source voltage for the nickel-contacted MoS_2 microribbon transistor, indicating ohmic contacts at room temperature.[43] Figure 3c shows a nonlinear dependence of drain current on drain-source voltage for the nanoribbon device before ALD passivation. Since the contacts on the original device did not change, this indicates that a Schottky barrier was created between the MoS_2 microribbon channel and the nanoribbon channel. Figure 3d shows a linear dependence of drain current on drain-source voltage for the nanoribbon device after ALD passivation, indicating a reduction of the Schottky barrier height. Our hypothesis for this behavior is that the Fermi level of nanoribbons is lower than that of microribbons, as the nanoribbons were more heavily p-doped by a higher ratio of edge defects and adsorbates,[9,44−47] which creates a Schottky barrier between each pair of microribbon channel and nanoribbon channel. After ALD passivation, edge adsorbates were reduced, so the Schottky barrier height decreased.

Next, we compare the electronic behavior of different nanoribbon transistors, summarized in Table 1. The range in the extrinsic field-effect mobility was 0.36−8.53 $cm^2/(V\ s)$, the range in the current on/off ratio was 10^3 −10^6, and the range in the subthreshold swing was 5.1−12.8 V/dec. In comparison, 5−15 nm thick multilayer MoS_2 nanoribbon devices reported in the literature had a mobility of 1.25−31 $cm^2/(V\ s)$, a current on/off ratio of 10^5−10^7, and a subthreshold swing of 1−10 V/dec.[9−11] Considering that Coulomb scattering is weaker for thicker channels due to an increased interaction distance between interfacial Coulomb impurities and charge carriers in the channel,[48] our monolayer nanoribbon devices have reasonable electrical properties compared with published values for multilayer nanoribbon devices. Finally, both Device A and Device C exhibited a current on/off ratio larger than 10^4, which is much higher than that of graphene nanoribbon FETs of a similar width[49] and comparable with that of 1 nm wide graphene nanoribbon FETs.[50]

To probe the impact of nanoribbon width on device performance, Figure 4 compares the transfer characteristics of two unpassivated nanoribbon devices that were fabricated on the same MoS_2 flake: a 30 nm wide device (Device A) and a 60 nm wide device (Device C). Device A had a field-effect mobility of 0.12 $cm^2/(V\ s)$, a current on/off ratio of 1 × 10^4, and a subthreshold swing of 6.5 V/dec, while Device C had a

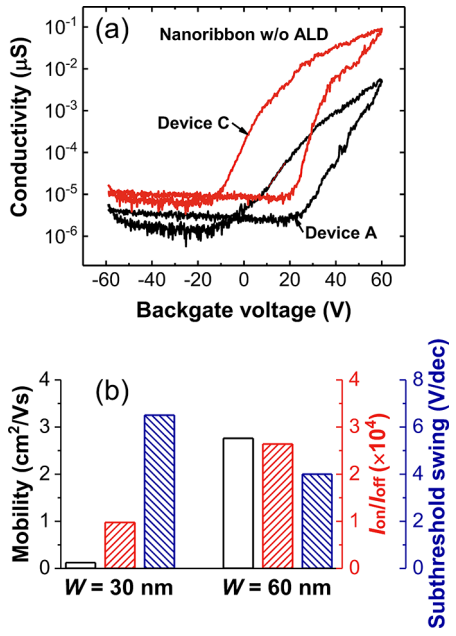

Figure 4. (a) Transfer curves of nanoribbon Device A (W = 30 nm) and Device C (W = 60 nm) before ALD passivation. V_{ds} = 1 V. (b) Comparison of the mobility, on/off ratio, and subthreshold swing of the two widths.

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field-effect mobility of 2.76 $cm^2/(V\ s)$, a current on/off ratio of 3×10^4, and a subthreshold swing of 4.0 V/dec. Device A had a smaller mobility and a lower on/off ratio than Device C, which may be explained by a more prominent role of edge roughness in narrower nanoribbons. In addition, Device A had a larger subthreshold swing than Device C, which indicates that narrower nanoribbon devices have a higher density of interface traps.

Finally, we studied the effect of nanoribbon patterning and ALD passivation on a threshold voltage. Threshold voltage V_T was extracted by linear extrapolation[51] for the reverse sweep at V_{ds} = 0.1 V, as shown in Figure 5. Although the threshold

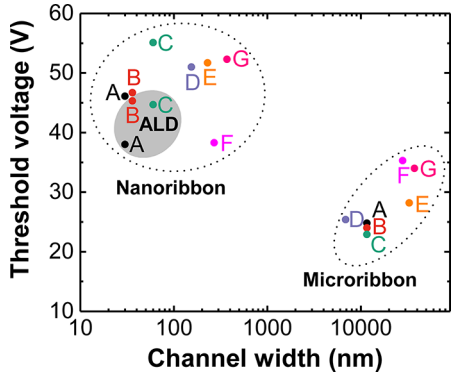

Figure 5. Threshold voltage as a function of channel width of all of the devices listed in Table 1. Nanoribbon devices after ALD passivation are shown in the gray zone.

voltage of the microribbon devices varied widely, all of the threshold voltages increased after nanoribbon patterning, consistent with the observed positive threshold voltage shift in multilayer (9−18 layers) MoS_2 nanoribbon transistors.[9] On average, the threshold voltage increased by 21 V after nanoribbon formation, likely due to carrier depletion by surface adsorbates (e.g., water).[9,11,52] After ALD passivation, the threshold voltage of all three nanoribbon transistors (Devices A, B, and C) decreased, which can be ascribed to reduced adsorbates.[38]

In summary, we demonstrated the fabrication of single-layer MoS_2 nanoribbon transistors with a channel width as narrow as 30 nm, by depositing a polymer etch mask with a heated AFM tip on prefabricated microribbon transistors to create ultra-narrow channel transistors. Of all of the fabricated nanoribbon devices, with a width ranging from 30 to 370 nm, the mobility ranged from 0.36 $cm^2/(V\ s)$ to 8.53 $cm^2/(V\ s)$, the on/off ratio ranged from 1×10^3 to 1×10^6, and the subthreshold swing ranged from 5.1 V/dec to 12.8 V/dec. We examined the electrical properties of the device at each stage of fabrication and found that the electrical properties (mobility, on/off ratio, and subthreshold swing) degrade after nanoribbon formation, while ALD passivation improves mobility and on/off ratio but degrades subthreshold swing. A change in the output characteristics indicates that a Schottky barrier was created after nanoribbon formation, and the Schottky barrier height was reduced after ALD passivation. By comparing a 30 nm wide device with a 60 nm wide device that was fabricated on the same MoS_2 flake, we found that the narrower device had a smaller mobility, a lower on/off ratio, and a larger subthreshold swing. We also observed that the threshold voltage increased after nanoribbon formation and decreased after ALD passivation.

Several steps could be taken to further improve the electrical performance of the MoS_2 nanoribbon transistors. First, the MoS_2 could be encapsulated before fabrication, perhaps with layers of hBN, which would reduce MoS_2 exposure to contaminants during processing.[53,54] The hBN could also be used as the gate dielectric material. Compared to SiO_2, hBN has fewer Coulomb impurities and traps and is atomically flat.[48] Second, the contacts could be selected to have a lower work function that would result in a reduced contact resistance and improved extrinsic field-effect mobility.[55−57] Recent articles have reported good contacts to MoS_2 using ultra-high-vacuum metal deposition[59] or SPL-based fabrication,[58,59] both of which would be highly compatible with the present work. Third, the devices could be smaller. The ultimate resolution of tDPN depends on ink type, surface chemistry, and tip shape.[23,32,60] For instance, deposition of 10 nm wide nanoparticle rows has been demonstrated with tDPN,[61] which could potentially serve as an etch mask for nanoribbon fabrication. The channels could be shorter as well in order to reduce channel resistance. Finally, since scanning probe lithography can be parallelized to scale up,[62−64] we envision that the entire fabrication process consisting of CVD growth, optical lithography, and SPL can be applied to manufacture ultrascaled MoS_2 devices at the wafer scale.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.9b00271.

AFM image and Raman spectrum of MoS_2; Raman spectra of the MoS_2 channel after tDPN; AFM topology of PMMA mask; SEM images of Devices A and C; device measurement; electrical performance of Devices A and B (PDF)

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Notes

The authors declare no competing financial interest.

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