High-k dielectric Al$_2$O$_3$ nanowire and nanoplate field effect sensors for improved pH sensing

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Abstract Over the last decade, field-effect transistors (FETs) with nanoscale dimensions have emerged as possible label-free biological and chemical sensors capable of highly sensitive detection of various entities and processes. While significant progress has been made towards improving their sensitivity, much is yet to be explored in the study of various critical parameters, such as the choice of a sensing dielectric, the choice of applied front and back gate biases, the design of the device dimensions, and many others. In this work, we present a process to fabricate nanowire and nanoplate FETs with Al$_2$O$_3$ gate dielectrics and we compare these devices with FETs with SiO$_2$ gate dielectrics. The use of a high-k dielectric such as Al$_2$O$_3$ allows for the physical thickness of the gate dielectric to be thicker without losing sensitivity to charge, which then reduces leakage currents and results in devices that are highly robust in fluid. This optimized process results in devices stable for up to 8 h in fluidic environments. Using pH sensing as a benchmark, we show the importance of optimizing the device bias, particularly the back gate bias which modulates the effective channel thickness. We also demonstrate that devices with Al$_2$O$_3$ gate dielectrics exhibit superior sensitivity to pH when compared to devices with SiO$_2$ gate dielectrics. Finally, we show that when the effective electrical silicon channel thickness is on the order of the Debye length, device response to pH is virtually independent of device width. These silicon FET sensors could become integral components of future silicon based Lab on Chip systems.

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1 Introduction

Silicon based biosensors have proven to be extremely useful tools for a variety of bio-analytical applications. After the first introduction of the adaption of a standard Metal-Oxide-Semiconductor Field Effect Transistor (MOS-FET) for physiological measurements in 1970 (Bergveld 1970) and the initial demonstration of the detection of pH (Bergveld 1972), Ion Sensitive Field Effect Transistors (ISFETs) have been used for a variety of other applications, such as the detection of various proteins (Bergveld 1991; Kruise et al. 1992), the indication of immunological reactions (Schasfoort et al. 1989), and the monitoring of cell activity (Lehmann et al. 2000). The physics of sensor operation have been well studied, and detailed analytical models combining electrochemical theory of electrodes in fluid with standard semiconductor theory have been developed (Bergveld 2003; Nair and Alam 2006; Squires et al. 2008; vanHal et al. 1996).

Use of VLS (Vapor-Liquid–solid)-grown nanowires as FETs for ultrasensitive, label-free sensors of both buffer pH and proteins in a fashion similar to previously used ISFET sensors was first demonstrated in 2001 (Cui et al. 2001). The device sensitivities were found to be much higher than counterpart ISFET sensors (down to 10 pM for streptavidin), and are generally attributed to the increased surface to volume ratios and the effect of increments in surface charge (Nair and Alam 2008). Subsequently, reports have shown detection of various molecules and processes, including DNA (Bunimovich et al. 2006; Hahm and Lieber 2004; Fritz et al. 2002), miRNA (Zhang et al. 2009), PNA (Zhang et al. 2008a), cancer biomarkers (Patolsky et al. 2006b; Stern et al. 2007a; Zheng et al. 2005), viruses (Patolsky et al. 2004), neuronal signals (Patolsky et al. 2006a), and cell response to various stimuli (Cohen-Karni et al. 2009; Stern et al. 2008). Efforts have been made to study parameters such as the ionic strength of the buffer (Bunimovich et al. 2006; Stern et al. 2007b), the effect of charge distance from the surface (Zhang et al. 2008b), the effect of biasing voltages (Elibol et al. 2008; Gao et al. 2010), and the effect of device width (Elfstrom et al. 2007). However, much opportunity still exists for exploration, especially with regards to the choice of the gate dielectric material of such FET biosensors. In this work, we present a novel process to fabricate nanowire and nanoplate FETs with Al_2O_3 gate dielectrics and we compare these devices with FETs with SiO_2 gate dielectrics. Though other works have shown the use of high-k dielectrics to improve nanowire FET characteristics (Bhowmick and Alam 2008; Gnani et al.

2007; Kim and McIntyre 2006; Zhu et al. 2009), to our knowledge this is the first report of a high-k dielectric used for physiological sensing applications. We also demonstrate that devices with Al_2O_3 gate dielectrics exhibit superior sensitivity to pH when compared to devices with SiO_2 gate dielectrics. Finally, we show that when the silicon channel thickness is on the order of the Debye length, devices with widths varying from 50 nm up to 2 μm exhibit similar response to changes in pH.

2 Theory

Fundamentally, for traditional MOSFETs, ISFETs and nanoFETs, the change in channel charge resulting from potential changes at the oxide/fluid interface is given by:

$$\Delta\sigma_{Silicon} = -C_D\Delta\psi_0 \approx -\frac{\varepsilon_D\varepsilon_0}{t_D}\Delta\psi_0$$

where C_D is the dielectric capacitance, $\Delta\Psi_0$ is the change in surface potential at the oxide/fluid interface, ε_D is the dielectric constant of the gate dielectric (3.9 and 9 for SiO_2 and Al_2O_3, respectively) (Robertson 2004), and t_D is the thickness of the dielectric. The coupling of changes in potential at the surface to changes in charge in the silicon, given by the dielectric capacitance, is a critical factor that ultimately determines device sensitivity. To increase this coupling, either the thickness of the gate dielectric can be reduced or a material with higher dielectric constant can be used. For example, the recurrent theme with traditional SiO_2 MOSFET devices was to reduce the gate oxide thickness continuously until undesirable gate leakage currents crippled device operation (Muller et al. 1999). When similar devices are used in ionic fluids as is the case with FET biosensors, these leakage issues are even further exacerbated. Thus, a logical solution to this problem is to use thicker gate dielectrics with higher dielectric constants for devices which exhibit similar if not higher sensitivities when compared to silicon dioxide devices. The increased thickness of these high-k dielectric devices results in robust devices that are much less susceptible to gate leakage issues. Al_2O_3 is known to be a good compromise between available high-k dielectric due to a dielectric constant that is higher than that of SiO_2 without substantially sacrificing the band gap of the oxide, which is another important consideration for reducing gate leakage currents (Robertson 2004).

Our work here demonstrates the first such use of a high k-dielectric as the gate oxide for nanowire biosensor applications. We use pH sensing as a benchmark to study the effect of three critical parameters on the device performance using experimental results and supporting simulations—the employed gate dielectric, the use of a

back gate, and the device width. We first present the novel fabrication process and electrical characteristics of the Al_2O_3 devices. We demonstrate that our devices are stable and operate in fluidic environments for up to 8 h, quantified by threshold voltage stability and leakage current characterization. In addition, we performed a robustness comparison of the Al_2O_3 devices and more typical SiO_2 devices to show that the high-k dielectric devices exhibit better functionality over many electrical sweeps in fluidic environments. This is primarily due to the possibility of increasing the thickness of high-k device gate dielectrics without compromising sensitivity. Next, we discuss how the back gate bias condition can be optimized to lower the effective electrical thickness of the device, thereby enhancing sensitivity. This is a general technique that can be used for any gate dielectric or sensing platform that employs a back gate structure. This technique was then used to perform a direct comparison of the observed pH response of 150 Å thick Al_2O_3 devices to 100 Å thick SiO_2 devices. The high-k dielectric devices exhibited an average improvement of pH sensitivity over their counterpart SiO_2 devices of around 1.5. Lastly, we perform a comparison of the pH responses of Al_2O_3 devices with identical characteristics except for differing widths. We show that when using the back gate bias optimization technique, pH response is virtually independent of device width. This opens the possibility of the use of microscale devices that are much easier to fabricate with the use of standard lithography.

3 Materials and methods

3.1 Device fabrication

Top down fabrication was utilized in this work to create the silicon nanoFET devices. Briefly, the fabrication flow began with bonded Silicon on Insulator (SOI) wafers, doped p type at $10^{15}/cm^2$ with a buried oxide thickness of 1,450 Å and top silicon thickness of 550 Å. After dry oxidation and subsequent wet oxide etch to thin down the top silicon layer to approximately 300 Å, electron beam lithography was used to define the nanowires and other small features, followed by liftoff of chrome to form the first hard mask. Next, optical lithography was used to define all of the larger features, such as the nanoplates and mesas to make contact to the nanowires. After another chrome evaporation and liftoff, the entire hard mask over the active silicon layer was complete (Fig. 1(a), part 1). Next, the active silicon layer was formed by wet etching away the top silicon with TMAH using the chrome patterns as a hard mask (Fig. 1(a), part 2). After doping the source and drain regions with boron (simulated doping $\sim 10^{19}/cm^3$), the fabrication process was split to form different gate

dielectrics. For silicon dioxide devices, the device was dry oxidized to controllably grow ~ 150 Å thick SiO_2. For aluminum oxide devices, the device was deposited with 75 cycles of atomic layer deposition (ALD) Al_2O_3, which results in ~ 150 Å thick Al_2O_3 (Fig. 1(a), part 3). At this point, any dielectric that can be deposited using an ALD process can be employed instead of aluminum oxide. Following the gate dielectric formation, the devices were annealed in forming gas to remove interface states. Via holes were etched into contact regions, and 250 Å/750 Å thick titanium/platinum was patterned to make contact to the source and drain regions of the devices (Fig. 1(a), part 4). A rapid thermal anneal was then performed at 550°C in a N_2 environment to reduce the contact resistance at the source and drain regions of the devices. Next, a 4,000 Å thick passivation layer of PECVD nitride was deposited over the entire wafer. Optical lithography and a dry CF_4 RIE etch were then used to etch the passivation layer directly over the device active area (Fig. 1(a), part 5). Al_2O_3 serves as an excellent etch stop during this etch back (etch selectivity of 60:1 for Si_3N_4:Al_2O_3) (Venkatesan et al. 2009), allowing for a uniform and well characterized etchback step. For SiO_2 devices, the etchback step needed to be timed carefully to ensure that the top gate SiO_2 was not damaged. The resulting SiO_2 gate oxide was measured via cross sectional SEM, and was found to be around 100 Å thick. During this step, the passivation layer over a platinum electrode close to the devices was also etched to expose the on-chip fluid gate. Top view SEMs of the devices are shown in Fig. 1(b), including zoomed in views of patterns of silicon nanowires, mesas used to connect to the devices, the etchback window to expose the devices, and the metal interconnects used to make the electrical contact. Cross sectional SEMs of both wire devices (Fig. 1(c)) and plate devices (Fig. 1(d)) show good insulation quality, which contributes to the stability of the devices in fluid.

3.2 Electrical measurements

4 mm×9.5 mm chips were placed into ceramic packages (Global Chip Materials 28 pin lead sized brazed package) as shown in Supplementary Fig. 2. Microfluidic channels were aligned to the chip using a mask aligner, and individual devices were contacted using wire bonding to the package. Teflon tubing was inserted into the ends of the channel, and the entire setup was covered with slow drying epoxy to insulate the devices and to mitigate fluid leakage issues. The entire ceramic package was then placed into a custom designed PC board connected to a computer that could individually address any of the devices that were wire bonded. Fluid was exchanged using the tubing and syringe pumps with syringes containing the various different solutions. Robinson buffer pH solutions were made using
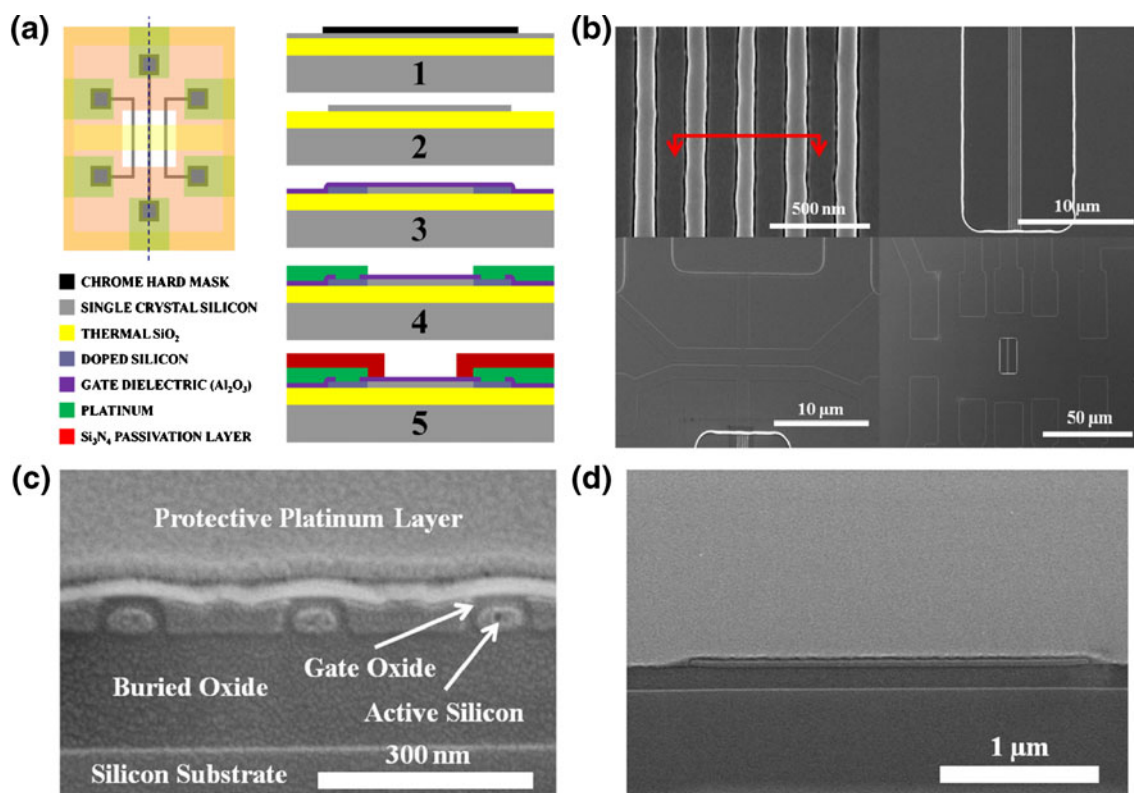
Fig. 1 Device structure. (**a**) Fabrication process for the Nano-FETs. *1*—Patterning of chrome hard mask via electron beam and optical lithography. *2*—Wet Etch of the active silicon area with TMAH. *3*—Deposition (Al_2O_3) or growth (SiO_2) of the gate dielectric. *4*—Deposition and patterning of platinum as the metal contact; contact is made with via holes into the silicon. *5*—Deposition of Si_3N_4 passivation layer, followed by etchback to expose the devices and the fluid gate. (**b**) Scanning electron micrographs of NW-FETs, demonstrating how mesas are used to make contact to the wires and to the metal traces. (**c**) SEM of a cross section of three NW-FETs (through the red line in part b). A protective platinum layer was placed over the cross section to prevent damage to the surface while taking the cross-section. (**d**) SEM of a cross section of a single nanoplate FET

1 mM acetic, 1 mM phosphate, and 1 mM boric with titrated HCl/NaOH to obtain the desired pH. All pH solutions were measured at the conclusion of the experiment to ensure that the pH had not changed significantly during the course of the experiment. Electrical current measurements and applied biases were controlled by a semiconductor parameter analyzer (Keithley 4200). Fluid gate biases were applied with an on-chip platinum electrode that made contact to the solution. Back gate biases were applied using the conductive platform of the ceramic package which made contact to the backside of the FET dies.

3.3 Carrier simulations

To obtain the carrier concentration profile inside the silicon channel as a function of the back gate bias, we used Medici with the two-dimensional planar structure. We modeled the electrolyte between fluid gate and top oxide as an insulator with thickness of 5 nm and dielectric constant of water (78.5 in the simulation). Since we used 5 mM electrolyte in the experiment, the corresponding Debye length (~5 nm)

can be reasonably used for the thickness of electrolyte layer. We also assumed that the fluid gate bias is negative (−1 V in the simulation), and the OH surface group is a negative (−10^{13} cm^{-2} in the simulation) fixed charge on the top oxide surface since the usual range of electrolyte pH is higher than the point-of-zero charge (pH$_{pzc}$) of SiO2 surface, which is equal to 1–3. To see the effect of the back gate bias, we used two different values of V_{BG} for the simulation: −7 and +3 V.

4 Results and discussion

The schematic used for electrical testing of the devices is shown in Fig. 2(a). A constant potential is applied between the source and drain, and the current between these nodes is measured as either the back gate voltage or the fluid gate voltage is swept. The fluid gate voltage is applied via an on-chip platinum pseudo reference electrode that was patterned as part of the metallization step during fabrication. Because platinum is known to have a pH-dependent
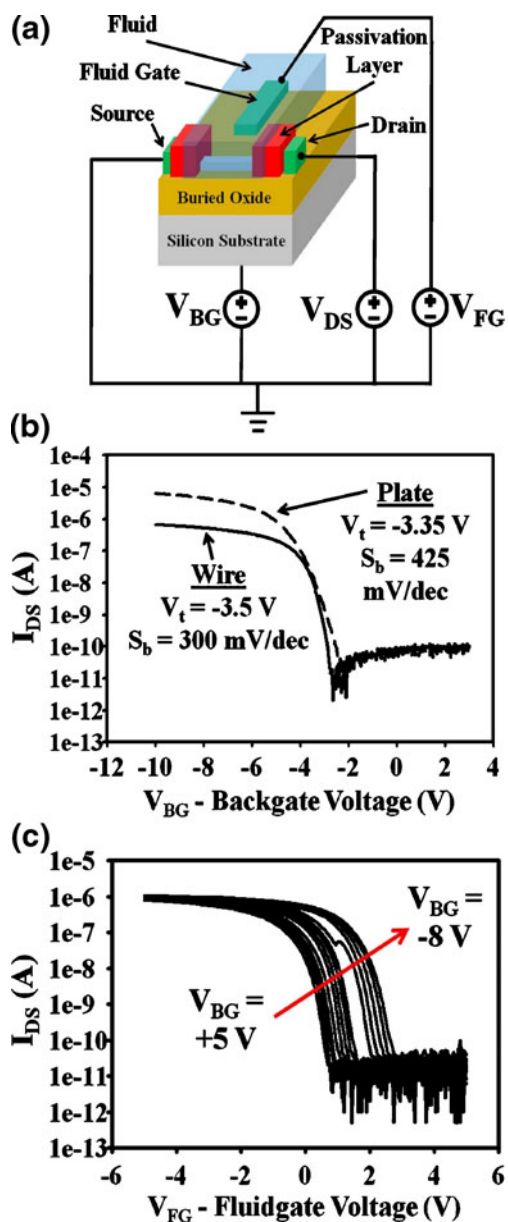
Fig. 2 Device operation. (a) Schematic demonstrating the measurement scheme for the nanoFETs. DC voltages are applied to the back substrate as a backgate (V_{BG}), to the on chip platinum reference electrode as a fluid gate (V_{FG}), and to the drain ($V_{DS}=1$ V for all experiments). Current is recorded from source to drain for the device. (b) Typical dry device operation for Al_2O_3 nanoFETs: both a 50 nm wide silicon nanowire and a 2 μm wide silicon nanoplate. Source-drain current (log scale) as a function of the applied backgate voltage. Included are the extracted threshold voltages and subthreshold slopes for the devices. (c) Measured source-drain current for an Al_2O_3 nanoFET in pH 7.4 0.01×PBS buffer solution the applied fluid gate is swept for many different applied backgate biases

Fermi level (Dankerl et al. 2008), we measured the open circuit potential between our platinum electrode and a reference Ag/AgCl electrode in Robinson buffers of various pH values with 10 mM of KCl. We observed a linear

decrease of about 41 mV/pH in the open circuit potential of the fluid gate, which can be viewed as additional sensitivity of the devices to pH (Supplementary Fig. 3). However, all figures in this work have been corrected for this effect, by subtracting the raw threshold voltage shifts by 41 mV per pH, and hence solely reflect surface potential shifts of the FET devices.

Initial Al_2O_3 device characterization was performed in air (without fluid on the devices) utilizing the back gate (V_{BG} in Fig. 2(a)). Both 50 nm wide nanowire devices and 2 μm wide nanoplate devices showed normal transistor behavior as the drain source current (I_{DS}) was measured while the back gate voltage was varied (Fig. 2(b)). Next, the devices were placed in a 0.01× Phosphate Buffered Saline (PBS) solution to measure the characteristics in fluid. The fluid gate voltage (V_{FG}) was swept from −5 to +5 V for backgate biases from +5 to −8 V (Fig. 2(c)). This demonstrates full double gate operation of the device; device current is modulated effectively by the fluid gate, and the different back gate biases correspond to shifts in the threshold voltage of the I_{DS}-V_{FG} curves. Very similar characteristics were observed with SiO_2 devices (Supplementary Information). Shifts in threshold voltage (of the I_{DS}-V_{FG} curves) were used for most experiments as a measure of changes in surface potential of the silicon to allow for comparisons that minimized the effect of device to device variation.

The devices were found to be very reliable for fluidic measurements, which was quantified by measuring the threshold variation, leakage currents, and device lifetimes in fluid. To determine the minimum observable shift in threshold voltage that could be considered real, we quantified the representative noise by measuring the threshold voltage of five Al_2O_3 nanowire devices as a function of time for up to 8 h, which is much longer than any typical experiment should take. The devices showed excellent threshold voltage stability over 8 h in fluid (Fig. 3 (a)), and also showed minimal changes in leakage currents even when tested over 10 months where the same device was exposed to fluid for about 30 min for each measurement (Fig. 3(b)). This device stability can be attributed to the proper protection of the electrical components from fluid with the silicon nitride insulating film as shown from the cross sections of the device (Fig. 1(c), (d), and Supplementary Fig. 1(b)). From the minimal threshold voltage drift, we found the minimum detectable change in threshold voltage for our system to be around 50 mV; any shifts in the raw data below this amount were not considered to be numerically significant. In addition, a study was performed directly comparing device robustness of the Al_2O_3 devices to typical SiO_2 devices. When the two sets devices were exposed to the same pH solutions and biasing conditions, a large percentage of the SiO_2 devices began to fail much earlier than the Al_2O_3 devices (Fig. 3(c)).
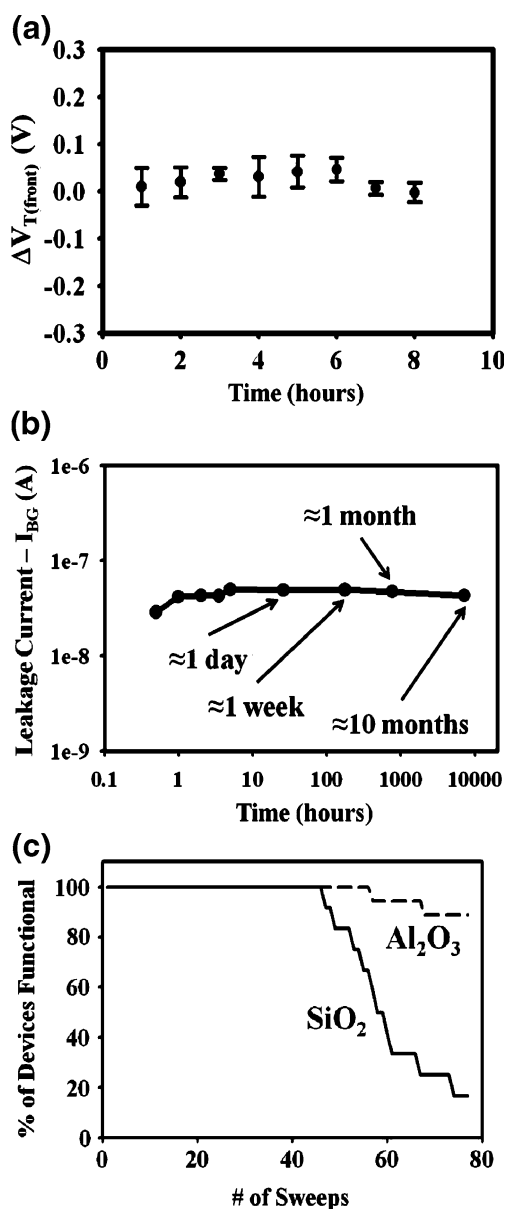
Fig. 3 Device Reliability. (a) Front threshold voltage versus time for 5 Al$_2$O$_3$ nanoFET devices demonstrating device stability. Very little shift in threshold voltage over time is observed for up to 8 h in Robinson buffer (pH 7.5). This allows us to determine our minimum detectable shift in threshold voltage (~50 mV). (b) Measured back to front leakage current as a function of time in 0.01× PBS for a 50 nm wide Al$_2$O$_3$ nanowire device. Devices are observed to maintain low leakage currents many months after initial measurement in fluid. (c) Device failure for SiO$_2$ and Al$_2$O$_3$ devices as a function of the number of sweeps (−5 V to +5 V) applied to the fluid gate at various backgate voltages in 10 mM, pH 7 Robinson buffer solution

Device failure was defined as either the presence of leakage currents higher than the source-drain current or as the lack of normal transistor behavior. The predominant factor responsible for this increase in device robustness is a thicker gate dielectric layer; with the Al$_2$O$_3$ devices a 150 Å thick gate dielectric could be used, whereas for the SiO2 devices a

thinner gate dielectric (~100 Å) was needed to see reasonable pH response.

The devices were first used to demonstrate the utility of the back gate during sensing. Recent reports singled out the careful tuning of the applied fluid gate bias to place devices in the subthreshold regime as a useful tool for maximizing the sensitivity of both pH and protein detection (Elibol et al. 2008; Gao et al. 2010). Fundamentally, the Debye length can be varied in the silicon channel. The Debye length dictates how far electric fields will penetrate into the silicon channel and is given by $\lambda_{Si} = (\varepsilon_{Si}\varepsilon_0 k_B T / \rho q^2)^{1/2}$, where ε_{Si} is the dielectric constant of silicon, ε_0 is the permittivity of free space, k_B is the Boltzmann constant, ρ is the net charge density, and q is the elemental charge ($\lambda_{Si} \sim 1$–2 nm for $\rho = 10^{18}$–10^{19} cm^{-3}). In response to charge modulation at the gate dielectric/fluid interface due to pH or protein binding events, changes in carrier concentration in the channel will occur principally within a Debye length away from the gate dielectric/silicon interface. By using the applied bias to reduce the net charge in the channel, the Debye length is increased, allowing for a higher percentage of the silicon channel to feel changes in charge at the surface, leading to increased sensitivity.

In this work, we show that the applied back gate bias can be similarly utilized to modulate the effective electrical device thickness. Distinct from a recent report, which demonstrated pH responses above the Nernstian limit by measuring shifts in the threshold voltage sweeping the back gate (Knopfmacher et al. 2010), our work uses the back gate only to optimize the silicon channel while sweeping the front fluidic gate potential. This method measures surface potential shifts at the sensing interface, which is of direct interest. The concept is analogous to accumulation mode fully depleted double-gated SOI MOSFETs (Iniguez et al. 1999; Jang and Liu 1999; Joachim et al. 1994), and is illustrated schematically in Fig. 4(a). Assuming that the front gate has been biased to place the top part of the channel into accumulation, changes in surface charge will only be felt a few nanometers into the top surface of the channel. If the back gate is biased to put the back of the channel into accumulation ($V_{BA} < -5$ V for most of the devices in this work), then a significant part of the 30 nm thick channel will conduct current that is insensitive to changes in surface charge (Fig. 4(a), left). Alternatively, if the back gate has been biased such that the channel is depleted except for the top accumulated surface (Fig. 4(a), right), the effective electrical thickness of the device has now been reduced to the order of a few nanometers. In this case, changes in surface charge directly influence the entire electrically active area of the channel, which will lead to increased sensitivity. The physical thickness of the device, at 30 nm, is much less than the theoretical maximum achievable depletion width for a 10^{15} p-type doped channel

Fig. 4 The influence of the applied backgate bias on pH sensing. **(a)** Schematic demonstrating the concept of using a backgate voltage to modulate the effective electrical thickness of the channel. On the left, when the back surface of the silicon is assumed to be in accumulation, a large percentage of the cross sectional area of the conductive channel (anything below the Debye length from the front) will not sense changes in charge at the dielectric-fluid interface. On the right, when the back surface is placed in depletion, the effective conductive thickness of the channel has been reduced so that the majority of the channel can detect charge. The fluid gate is assumed to be biased in both cases to place the front surface in accumulation. **(b)** Simulated carrier densities in the channel of nanoFET devices for the case of back accumulated ($V_{BA}=-7$ V) and back depleted ($V_{BD}=-4$ V). The front gate was accumulated, at $V_{FG}=-1$ V, and the concentration of charged sites on the surface was taken to be $N_s=10^{13}$ cm^{-2}. **(c)** Experimental data showing the percentage change in current from the current at pH 2.6 for three 50 nm wide Al$_2$O$_3$ nanowire devices at two different backgate voltages in accumulation and depletion ($V_{BG}=-7$ V and $V_{BG}=-4$ V). A higher sensitivity is noted in the case of the back depletion. Error bars were calculated as the standard deviation of the percentage error for the three employed devices

(~800 nm). Medici, a 2D device simulation tool, was used to simulate the net carrier concentration as a function of the vertical position in the channel (Fig. 4(b)), with an applied front gate voltage of $V_{FG}=-1$ V and two different back gate voltages, $V_{BG}=-7$ V and -4 V. A silicon surface carrier concentration on the order of 10^{18} at the top channel/gate dielectric interface was simulated for both back gate accumulated and depleted. However, when the back silicon was accumulated, an additional channel forms at the back gate which will be insensitive to charge changes at the front, thus reducing overall sensitivity. The expected trends were then confirmed experimentally. Selection of the appropriate buffer for use during pH experiments is very important. Robinson solutions were used because of the capacity as a universal buffer to maintain pH over a large range of pH values. In addition, all solutions were measured after the experiment to confirm that the solutions maintained the pH values that were plotted. As the solutions slowly flowed over the surface of the 50 nm wide Al$_2$O$_3$ devices, drain source current was measured as a function of applied fluidic gate bias at two fixed back gate biases to put the back silicon first in accumulation then depletion. An example of a typical result is shown in Fig. 4(c), at an applied fluid gate of $V_{FG}=1.5$ V. When the back silicon was placed into accumulation, at $V_{BA}=-4$ V, a distinct increase in current of around 100% of the original value was observed when varying the pH from 2.6 to 8.3. However, when the back was placed into depletion ($V_{BD}=-7$ V), a far higher change was observed: up to 700% increase in current, which matches the predictions of the Medici simulations.

Next, we used the back gate optimization technique to compare the performance of devices with Al$_2$O$_3$ gate dielectric against SiO$_2$, which has been traditionally used in nanoscale field effect biosensors. Al$_2$O$_3$ films are
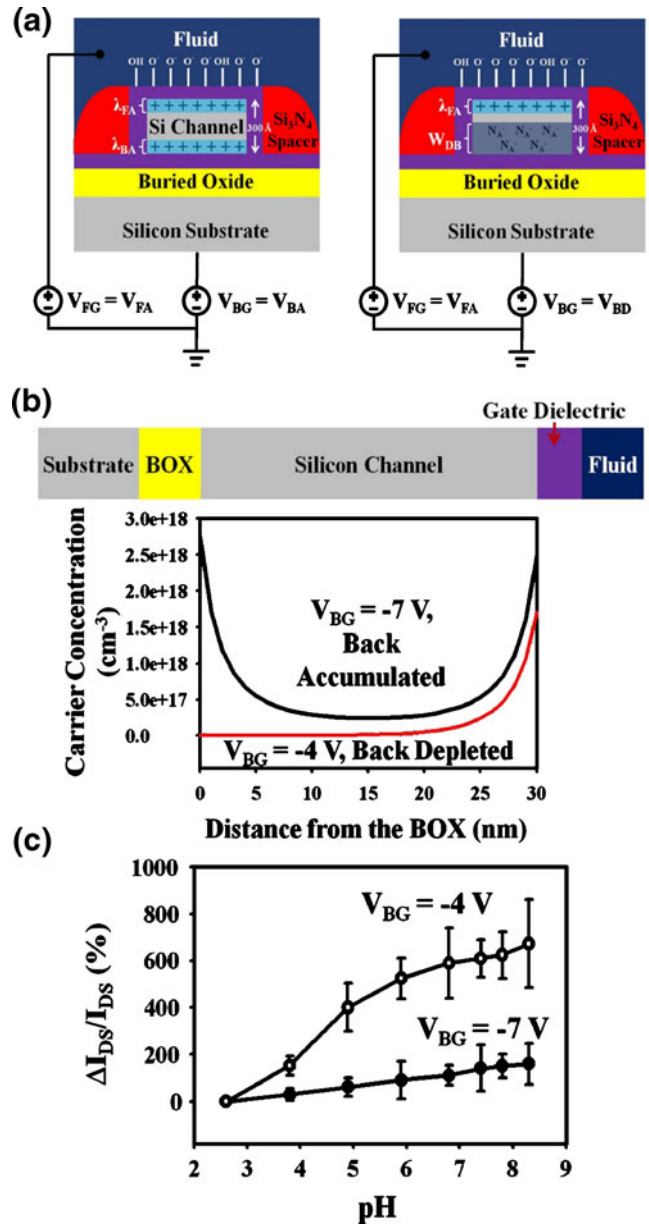
expected to have greater sensitivity to pH changes than their SiO$_2$ counterparts. When biosensor device sensitivity is defined as $S=\Delta G/G_0$, Nair et al. showed that device sensitivity is linearly proportional to ε_D, and can be written as (Nair and Alam 2008):

$$S = \frac{2\varepsilon_D\varepsilon_0\psi_0 N(t)}{qa^2 N_D \log\left(1+\frac{t_D}{a}\right)}$$

where $N(t)$ is the density of charge states at the surface, a is a geometry parameter, N_D is the doping of the silicon, and t_D is the thickness of the gate dielectric. The linear relationship here between the dielectric constant and the predicted sensitivity is a direct result of increase in the oxide capacitance as was discussed earlier.

In addition, for pH sensing, the change in surface potential for an ISFET sensor (which is directly relevant here) is given by (Bergveld 2003):

$$\Delta\psi_0 = \frac{-2.3\frac{RT}{F}\Delta pH}{(2.3kT/q^2)(C_s/\beta_s)+1}$$

where C_s is the differential double layer capacitance (dependent mostly on the ion concentration of the solution) and β_s is the buffer capacity of the surface, which is known to be markedly higher for Al_2O_3 when compared to SiO_2 (Bergveld 2003). The sensitivity enhancement offered by an Al_2O_3 dielectric is thus two-fold: (1) the increase in the dielectric constant correlates to an increase in oxide capacitance, thereby enhancing the response, and (2) the buffer capacity of the surface of Al_2O_3 films is higher, which leads to a higher surface potential shift for Al_2O_3 devices.

We performed a side by side comparison of the silicon dioxide (100 Å gate dielectric) and the aluminum oxide devices (150 Å gate dielectric). The devices were optimized for back gate biasing conditions, and were placed into the Robinson buffer solutions of varying pH. At each pH, I_{DS} was measured as a function of V_{FG} for a constant V_{BG}. The threshold voltage for each curve was extracted using a constant current method (Supplementary Information). Results for three Al_2O_3 and three SiO_2 devices, all 50 nm in width and 30 nm thick, are shown in Fig. 5. The observed average sensitivity of threshold voltage shift per pH is approximately 1.5 times higher for the Al_2O_3 devices when compared to the SiO_2 devices, which is slightly higher than reported comparisons for ISFET devices, around 1.3 (Bergveld 2003). This increase in sensitivity is observed despite the fact that the Al_2O_3 devices had a thicker gate dielec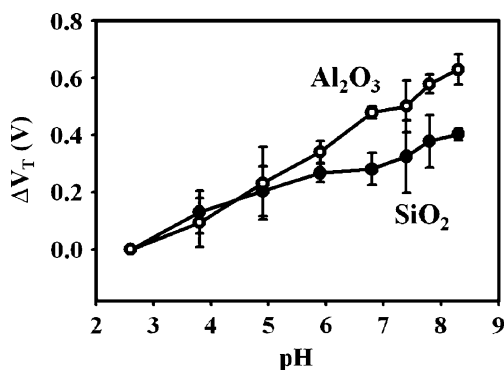tric which helps with robustness and reduction of leakage currents. In addition, the Al_2O_3 devices exhibit an average pH response (from pH 2.6 to 8.3) that is approximately 1.3 times higher than recent reports of the pH sensitivity of SiO_2 devices using a similar back gate structure (Knopfmacher et al. 2010). The error bars in Fig. 5 were obtained as an average of the results of three different devices, and are due mostly to device to device variation. Individual devices showed very high repeatability, with the capability of distinguishing pH changes down to 0.062 pH units (see Supplementary Information).

The Al_2O_3 devices were next used to investigate the effect of device width on sensitivity of pH detection, with and without back gate optimization. We found that for devices with a physical thickness of 30 nm, the devices showed very similar responses to changes in pH for a range of widths varying from 50 nm (nanowires) up to 2 μm (nanoplates). This is explained conceptually in Fig. 6(a).
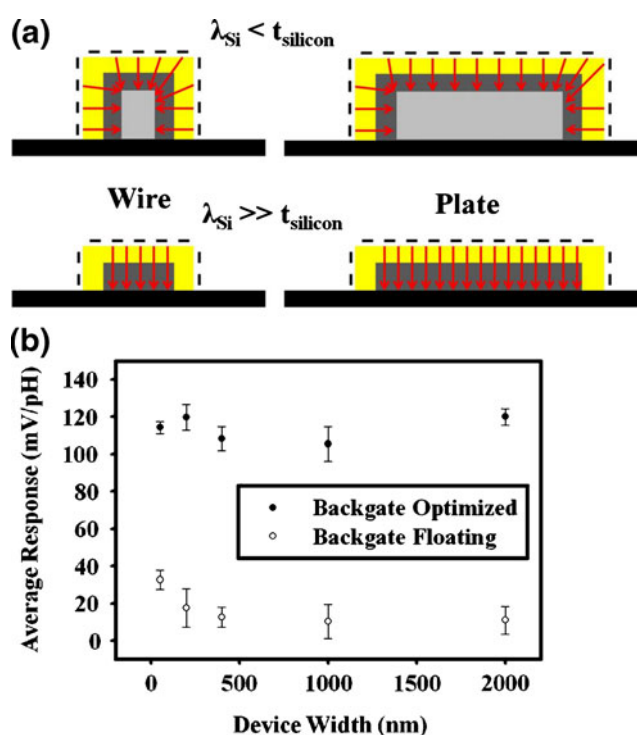

Fig. 6 Comparison of NWFET devices and nanoplate FET devices. (a) Schematic illustrating two separate cases: when the silicon Debye length is much less than the silicon thickness (*top*) and when the Debye length is much greater (*bottom*). A large difference in the% of the channel that can sense charge at the dielectric/fluid interface is noted for nanowire vs. nanoplate in the top case, whereas no difference is seen in the bottom case. (b) Average pH response (calculated by fitting a line to eight pH points) as a function of device width (50 nm, 200 nm, 400 nm, 1 μm, and 2 μm wide devices) in an experiment with both optimized back gate biases (*top*) and with the back gate left floating (*bottom*). The response is seen to be virtually independent of device width when the back gate is optimized, but a slight increase in response is seen when reducing device width in the case of the floating back gate. Error bars were calculated with three separate devices in each case

Fig. 5 Experimental comparison of pH-induced threshold changes using three Al_2O_3 NWFET devices and three SiO_2 devices. The Al_2O_3 devices demonstrate a higher sensitivity to pH, which is expected based on the difference in buffer capacities of the surfaces. Error bars were calculated using the standard deviation of the threshold voltage shifts of the three devices used in the study

When the thickness of the devices is much larger than the silicon Debye length (top) as previously reported (Elfstrom et al. 2007), changes in charge at the surface affect a much larger percentage of the cross-section of the device channel for a wire configuration (left) as compared to a plate (right), thus resulting in higher responses for the wire as compared to the plate. This is due primarily to the exposure of the sidewalls of a nanowire device, which allow for more of the channel charge to be modulated by the sidewall. However, for our devices, after back gate optimization, the effective electrical channel thickness is much smaller or on the same order as the silicon Debye length (Fig. 6(a), bottom). Changes in charge at the top surface affect the entire channel regardless of whether a nanowire or a nanoplate is used to measure response. In this case, very little dependence of sensitivity or response is expected on device width. This trend was observed experimentally for Al_2O_3 devices, by flowing Robinson buffers of different pH values over 50 nm, 200 nm, 400 nm, 1 μm, and 2 μm wide devices patterned on the same chip in close proximity. With the optimization of back gate bias conditions, we saw very little relationship between device width and the measured average pH response (Fig. 6(b), top), with a maximum deviation of less than 15% for all the device widths measured. However, when the back gate was left floating (making the device electrical thickness on the order of the physical thickness), a slight improvement in average pH response of around 300% could be seen when decreasing the device width from a 2 μm plate to a 50 nm wire (Fig. 6 (b), bottom). These results lend evidence to the claim that the primary concern for increasing pH sensitivity is maintaining a device electrical thickness that is much smaller than the silicon Debye length. Decreasing device width beneath the lithographical limit often results in increased cost and complexity of processing and may be unnecessary if proper biasing schemes are applied, in the case of pH sensing.

5 Conclusions

In summary, we have explored critical parameters that could be used to optimize the sensing of pH changes by field effect sensors. We have demonstrated a top-down fabrication process that incorporates a new dielectric material, Al_2O_3, suggesting the possibility that a wide variety of other high k-dielectrics can also be utilized in nanowire field effect sensors. The use of high-k dielectric materials improves both sensitivity and robustness by allowing for the use of a thicker gate dielectric, which reduces gate leakage issues in fluid. Both the Al_2O_3 and SiO_2 devices showed normal stable transistor operation. By applying a potential to the back gate we were able to thin the effective electrical thickness of the devices to a few nanometers, which dramatically increases the response of the devices. The Al_2O_3 devices outperformed their counterpart SiO_2 devices by an average sensitivity improvement of 1.53, matching theoretical expectations. Lastly, an on-chip comparison of devices of varying width from the nanoscale to the microscale showed that when the effective device thickness is on the order of the silicon Debye length, response to changes in pH is relatively independent of device width.

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