A Complementary Bipolar Technology Family With a Vertically Integrated PNP for High-Frequency Analog Applications

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***Abstract*—Silicon complementary bipolar processes offer the possibility of realizing high-performance circuits for a variety of analog applications. This paper presents a summary of silicon complementary bipolar process technology reported in recent years. Specifically, an overview of a family of silicon complementary bipolar process technologies, called Vertically Integrated PNP (VIP™[1]), which have been used for the realization of high-frequency analog circuits is presented. Three process technologies, termed VIP-3, VIP-3H, and VIP-4H offer device breakdowns of 40, 85, and 170 V, respectively. These processes feature optimized vertically integrated bipolar junction transistors (PNPs) along with high performance NPN transistors with polycrystalline silicon emitters, low parasitic polycrystalline silicon resistors, and metal–insulator–polycrystalline silicon capacitors. Key issues and aspects of the processes are described. These issues include the polycrystalline silicon emitter optimization and vertical and lateral device isolation in the transistors. Circuit design examples are also described which have been implemented in these technologies.**

I. Introduction

ANALOG circuits are an integral part of any electronic system in use today and will find increasing use in applications where high voltages or an interface to the outside world is required. With the increasing demands of higher performance, high speed, and low distortion operational amplifiers, circuit designers need higher performance complementary bipolar technologies specifically aimed for analog applications. Even though the complementary bipolar process technology drives a smaller part of the market than core high-density complementary metal-oxide semiconductor (CMOS) technology, it still constitutes a very important segment of the overall integrated circuit market. Specifically, a high-performance bipolar junction transistor (PNP) is very desirable in the signal path because it can offer the opportunity for designing push–pull circuits and active loads for analog applications. In addition, high performance PNPs can enhance the circuit performance as drivers in the output stages by reducing the supply current. The key requirements for analog process technology are the required breakdown voltages for specific applications, high βxVa product, high f_T and $f_{\max}$ for high speed applications, and low noise for both NPN and PNP devices. Other important requirements for the success for any technology are, of course, low cost and manufacturability.

Unlike MOS process technology, bipolar process technology is typically not truly complementary. In most cases, only vertical NPN bipolar junction transistors are optimized and PNP bipolar junction transistors are usually "free," i.e., no added processes steps are needed. The two main types of these "free" PNP devices are i) substrate PNP and ii) Lateral PNP. Substrate PNPs are made from the NPN p-type base, n-type collector, and p-type substrates. Hence these devices are not isolated from each other and are connected through the substrate. The lateral PNP devices are made using the p-type extrinsic base, n-type collector, and the p-type extrinsic base of the NPN. The base contact is provided by the NPN n+ buried layer. The word "lateral" refers to the direction of the current flow with respect to the wafer surface since in these devices the current flows laterally from the emitter to the collector, unlike in vertical devices where the current flows from the emitter down to the collector and the buried layer. The lateral device has a large base resistance and hence a poor f_T and $f_{\max}$, limiting its use in high frequency applications. Thus, both these types of devices are not suited for high frequency, switching, or high performance applications. Fig. 1 shows the three types of PNP devices possible in a NPN process.

The purpose of this paper is to discuss silicon complementary bipolar technologies and their applications. The complementary bipolar processes reported to date in literature are also summarized. In addition, a family of processes called VIP™ is described. Three processes with device breakdowns at 40, 85, and 170 V are described. Key process issues are described and circuit design examples are presented that utilize the unique features of these technologies.

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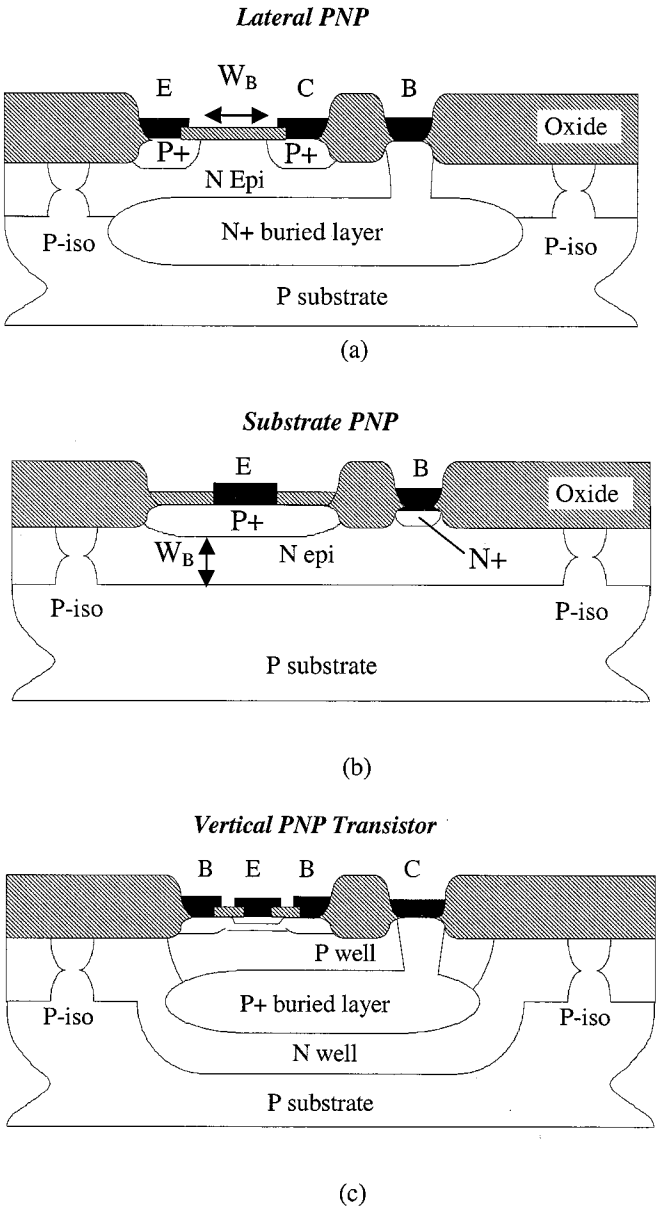

Fig. 1. The three types of PNP devices typically used in NPN BJT processes: (a) lateral PNP, (b) substrate PNP, and (c) vertical PNP.

II. Review of Complementary Bipolar Technologies

Many complementary bipolar technologies are reported in the literature from the late 1960s to very recently [1]–[38]. From its early inception, complementary bipolar processes have been used for realizing high performance analog circuits. In one of the earliest reports of the complementary bipolar technologies in 1968 [1], NPN and PNP devices were achieved in a monolithic structure by fabricating them in different wafers and then soldering the two wafers together face to face. The wafers were aligned within an accuracy of 1 mil (25 μm) by fitting metal bumps on one wafer into pockets on the other wafer. Subsequently, the two types of devices were fabricated within the single substrate for the first time [2]. This opened the way for integrated complementary bipolar device. Su *et al.* [3] used one extra diffusion to devise NPN and PNP devices with high current gain and low saturation resistance. Many authors subsequently reported integration of PNP devices and their optimization in NPN process, thus realizing complementary bipolar processes [4]–[9].

Since the early 1980s, there have been many reports of high performance complementary bipolar processes for analog applications. One of the first high voltage processes was described by Aull, *et al.* [10] with breakdown voltages of 60 V for telecom subscriber line interface circuits. The process produced vertical NPN and PNP devices with $BVceo$ of 60 V and β of about 100. Subsequently, a circuit for a line interface between two-wire subscriber loops and the low-voltage four-side of a telephone exchange was described using a complementary (C)-bipolar technology [11]. Low voltage and digital functions were provided in standard 60 V junction isolated process. The high voltage two-wire side of the subscriber circuit was built in a 200 V dielectrically isolated complementary bipolar technology. A process was also reported with vertically double diffused transistors in complementary islands with breakdown voltages of more than 350 V and f_T of 450 and 200 MHz for the NPN and PNP transistors, respectively [12]. A subscriber line interface circuit that includes battery feed, supervision, and hybrid was demonstrated using this technology. An ion-implanted base-emitter in a complementary bipolar process was reported with reduction in leakage currents from ion-implanted boron for the PNP emitter [13], [14]. In order to reduce parasitics, various authors have reported devices fabricated on silicon-on-insulator (SOI) wafers and trench isolation. Bonded and etched back SOI (BESOI) wafers have found significant use in these processes [15], [18]–[21], [26], [35]–[37]. SOI wafers make the process simpler, i.e., no n-wells are needed for the PNP device isolation, and the device size and parasitic capacitances are reduced. The use of trenches and SOI does increase the wafer cost and hence many junction isolated processes made in bulk wafers have also been reported [17], [23], [29], [30], [32], [34], [38].

III. VIP™ Process Details

In order to fulfill the need for high-precision and high-frequency analog circuits, a family of complementary silicon bipolar processes has been developed [29], [30], [35], [36]. Three technologies named VIP-3, VIP-3H, and VIP-4H are described in the following. These processes use a single polycrystalline silicon layer architecture for the base-emitter formation. VIP-3 and VIP-3H use junction isolation, whereas VIP-4H uses a dielectrically isolated process with trenches and BESOI wafers.

A. VIP-3

A high performance and low cost complementary bipolar technology has been developed for the realization of high-precision and high-frequency analog circuits [29]. The technology, referred to as VIP-3, offers transistors with typical BV_{ceo} for NPN and PNP transistors of 45 and 60 V, respectively, with other device specifications detailed in Table I. The technology uses deep junction isolation, a deep n-well for the PNP vertical isolation, twin buried layers, n-type epitaxial layer, combined with single-poly quasiself-aligned emitter/base transistor

TABLE I
LIST OF DEVICE PARAMETERS FOR THE VIP-3, 3H, AND 4H TECHNOLOGY. $A_e = 4 \times 20\ \mu\text{m}^2$

		VIP-3		VIP-3H		VIP-4H	
Paremeters	**Units**	**NPN**	**PNP**	**NPN**	**PNP**	**NPN**	**PNP**
β	-	100	65	120	60	80	50
Va	V	200	100	500	120	2400	800
Re	Ω	2.1	3.3	2.1	3.3	4.5	10.3
Peak f_T	GHz	3.1	2.4	2.0	1.6	1	0.9
Peak f_{max}	GHz	4.2	3.8	-	-	-	-
BVceo	V	45	60	85	95	185	200
BVcbo	V	50	60	115	105	220	220
BVebo	V	5.7	6.3	5.7	6.3	4.8	6.1
Cje	fF	196	110	198	206	302	249
Cjc	fF	89	190	150	237	151	114
Cjs	fF	483	630	604	652	100	100

structure with a minimum feature size of 2 μm. The process also offers n and p-type polycrystalline silicon resistors and polycrystalline silicon/oxide/metal capacitors. A cross-section view of the NPN and PNP devices is depicted in Fig. 2.

Process Flow: Fig. 3 shows the module process flow for the complementary bipolar process. The process begins on a p-type substrate into which phosphorus is implanted and driven to form the deep n-well for the PNP vertical isolation. Next, the n-type antimony buried layer for the NPN is implanted and driven. Since the collector resistance and hence the saturation voltage (V_{cesat}) needs to be minimized, heavily doped "sinker" regions need to be formed to access the buried layer from the top of the wafer. The epitaxial layer thicknesses are large for these voltage ranges and hence, only a sinker-down dopant region is not sufficient to connect to the buried layer. Thus, the n-type phosphorus sinker-up is formed by ion implantation. Next, boron implant is used to form the PNP buried layer regions and the isolation areas. A rapid thermal anneal cycle is performed prior to epitaxial growth to eliminate implant damage in the n-type sinker-up and PNP buried layer regions. Epitaxial deposition is performed in a reduced pressure, radiantly heated barrel reactor at 1080 °C. An n-type, 8.5 μm-thick epitaxial layer is grown.

Next, n-type and p-type sinker-down regions and p-well dopants are implanted in the epitaxial layer through a pad oxide. The formation of vertical PNP transistors, along with vertical NPN transistors, is a complex task due to the added requirement of the formation of the P well. In the VIP-3 process, an n-type epitaxial layer was grown and counter doped to form the P well of the PNP transistors. The counter doping requires a p-type dopant which needs to diffuse down to merge with the boron buried layer. Aluminum is a p-type dopant in silicon and has a diffusion coefficient that is about an order of magnitude higher than that of boron [41]–[44]. Boron implants were also used for the formation of the shallow region of the P well. Next, a nitride layer is deposited and defined for a standard LOCOS process. A diffusion/oxidation cycle is used to link the n-type sinker-up and n-type sinker-down regions and to link the PNP buried layer and p-type sinker-down regions.

After the sinker diffusion/LOCOS formation, intrinsic and extrinsic bases are implanted through a pad oxide into the silicon using photoresist masks. Windows through the pad oxide are opened and a polycrystalline silicon layer is deposited. The

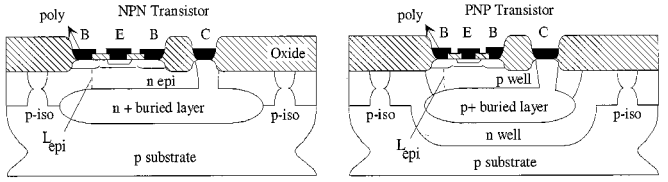

Fig. 2. Cross-sectional diagram of the VIP-3 and VIP-3H NPN and PNP transistor.

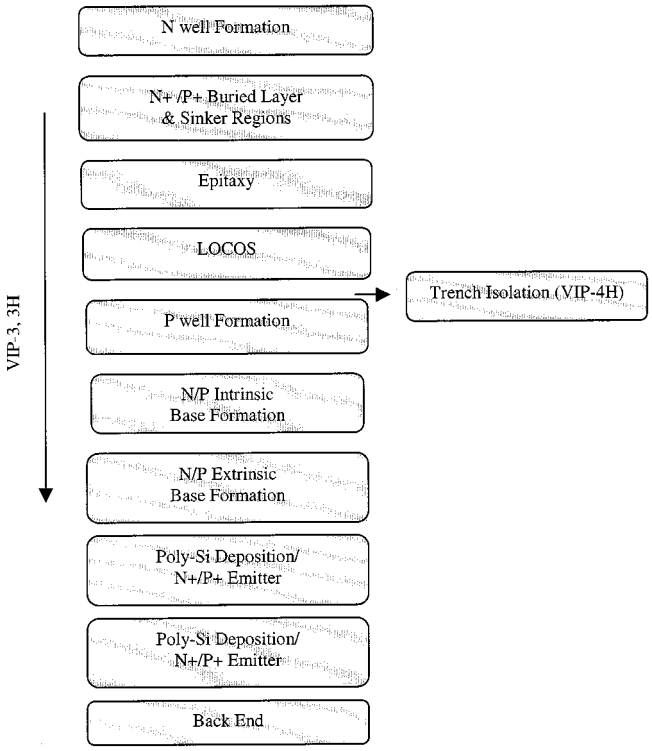

Fig. 3. Modular process flow for the VIP complementary bipolar technology.

wafer clean process prior to the polycrystalline silicon deposition consists of pirahana ($1:1\ H_2O_2 : H_2SO_4$) clean followed by a short exposure in 10 : 1 hydrofluoric acid. The wafers are then loaded in the CVD tube at 400 °C and the tube is pumped down to reduce oxidation prior to deposition. The temperature is then ramped to the final polycrystalline silicon deposition temperature. This scheme has been shown to provide consistent and repeatable electrical results, thus enhancing manufacturability of polyemitter bipolar process [39]. Following the polycrystalline silicon deposition, an RTA step is used to break any interfacial native oxide. The polycrystalline silicon layer is then implanted with boron and arsenic for the emitter regions. Furnace anneal cycles are finally used to diffuse the dopant from polycrystalline silicon into the monocrystalline silicon regions to form and activate the emitter and extrinsic base contact regions.

Electrical Results: Fig. 4 shows the I_c–V_{ce} characteristics of the VIP-3 NPN transistor, while Fig. 5 shows the I_c–V_{ce} characteristics of the PNP transistor. Fig. 6 shows the Gummel plot of both NPN and PNP transistors exhibiting constant gain over seven decades indicating excellent material and junction quality. The current gain (β), early voltage (V_a), collector-emitter breakdown voltage (BV_{ceo}), and junction capacitance for the NPN/PNP devices are listed in Table I. The higher PNP

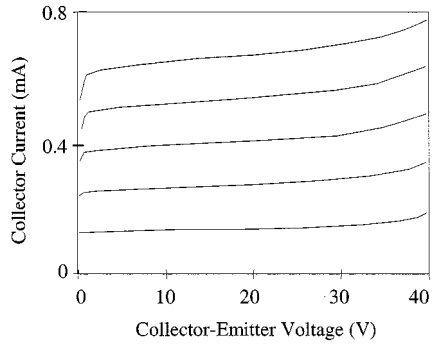

Fig. 4. I_c versus V_{ce} for a VIP-3 NPN device with area of $2 \times 20\ \mu\text{m}^2$; Ib steps of $1\ \mu$A.

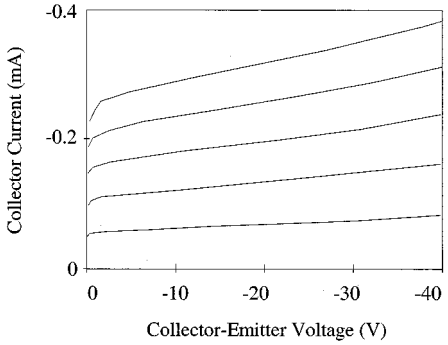

Fig. 5. I_c versus V_{ce} for a VIP-3 PNP device with area of $2 \times 20\ \mu\text{m}^2$; Ib steps of $1.5\ \mu$A.

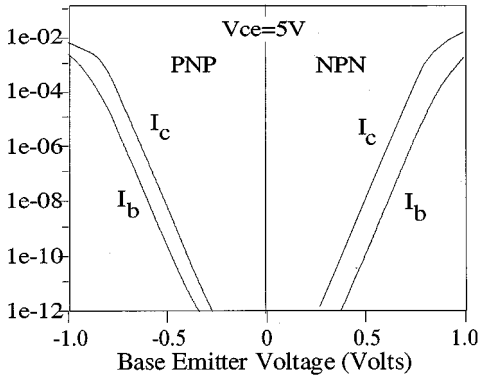

Fig. 6. Gummel plots for the VIP-3 NPN and PNP devices, area $= 2 \times 20\ \mu\text{m}^2$.

BV_{ceo} is attributed to the reduced susceptibility to avalanche breakdown [30]. It is to be noted that unlike many complementary processes, VIP-3 process offers PNP f_T being 77% to that of the NPN f_T, attributed mainly to p-well process design and optimization. The maximum oscillation frequency, $f_{\max}$, is obtained from the unilateral gain measurement. Note that the $f_{\max}$ values are in the GHz range even for $4 \times 20\ \mu\text{m}^2$ emitter and the values for the PNP are 90% of those of the NPN transistor.

B. VIP-3H

A high-performance and low-cost complementary bipolar technology has also been developed for the realization of high-precision, high-frequency, and high-voltage analog circuits for the monitor and CRT market. The process also achieves its high performance without the use of expensive modules such as trench isolation or bonded wafers.

Process Flow: The process flow is very similar to the VIP-3 process flow described previously, except that higher breakdown voltages are obtained by increasing the epitaxial layer thickness and increasing the resistivity. The final cross-section view of the NPN and PNP devices is very similar to the one depicted in Author inconsistent with math variables. Fig. 2.

To form the deep portion of the p-well, boron, and aluminum implantation and diffusion were used rather than MeV Boron implantation. The epitaxial layer thickness was increased to 13.5 μm and hence the thick n-type epitaxial layer has to be compensated to form the p-well for the PNP device. The key issues with aluminum are its very high diffusivity (an order of magnitude higher than boron) and low electrical activity, i.e., approximately, only 1/40 of the implanted dose becomes activated following the well drive [43], [44].

Electrical Results: The Gummel plots of the VIP-3H devices exhibited a constant gain over seven decades of current, indicating excellent material quality for both devices just as for the VIP-3 devices. The collector-substrate breakdown voltage was optimized using process and device simulators. The NPN-buried layer to p-type substrate breakdown is determined by the avalanche breakdown at the junction at the edge of the buried layer since that is where the field gradient is the highest and can be controlled by substrate doping. The PNP buried layer to p-type substrate breakdown requires a careful selection of the n-well doping to optimize the trade-off between the punch-through voltage in the n-well and avalanche breakdown at the periphery. If the n-well doping is low, then breakdown occurs due to punch-through of the n-well under the p+ buried layer. If the n-well doping is high, then avalanche breakdown occurs at the periphery.

The BV_{ceo} and BV_{ceo} were the other key breakdown values to be increased to greater than 85 V. Since BV_{ceo} is limited by BV_{cbo} according to $BV_{\text{cbo}} \cong BV_{\text{ceo}}\beta^{1/m}$, BV_{cbo} was optimized first. The BV_{cbo} is limited by the edge breakdown effects. A deeper extrinsic base results in a smaller junction curvature at the edges and hence, a higher breakdown. On the other hand, if the distance from the extrinsic base-collector junction to the buried layer is too small then BV_{cbo} will be limited by the reach-through of the depletion region to the buried layer. This collector-base depletion region reach-through sets the thickness of epitaxial layer.

BV_{ceo} is a function of the intrinsic or "planar" BV_{cbo} provided that the intrinsic BV_{cbo} breakdown is higher than the terminal BV_{cbo} limited by edge effects. This is the case for VIP-3H where due to the thicker epitaxial layer under the intrinsic base, the intrinsic BV_{cbo} is much higher than the terminal BV_{cbo}. The intrinsic BV_{cbo} could not be measured but was obtained using simulations as shown in Fig. 7. Also shown in Fig. 7 is the measured BV_{cbo} and BV_{ceo} for the NPN and PNP with the final optimized doping profiles. It should be noted that due to the up-diffusion of boron-buried layer, the distance L_{epi} for PNP is half than that for NPN. The BV_{cbo} for PNP is still high and this is attributed to the smaller impact ionization rate for holes as compared to electrons [40].

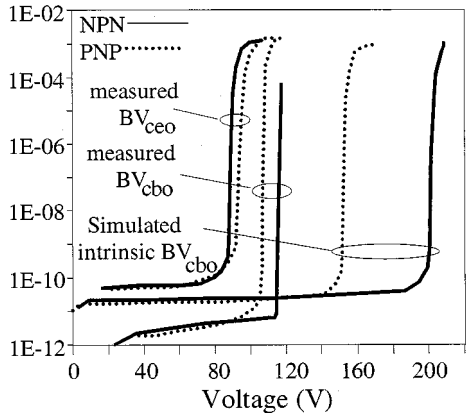

Fig. 7. VIP-3H NPN and PNP collector-base and collector-emitter breakdown voltages.

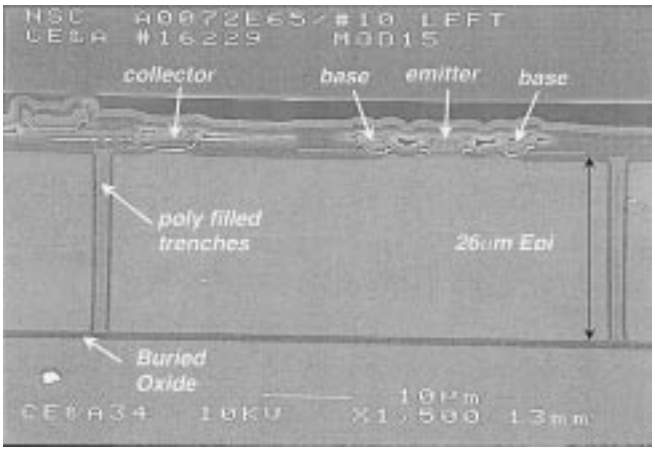

Fig. 8. Cross-sectional SEM of a VIP-4H transistor.

C. VIP-4H

VIP-4H is a high-speed complementary bipolar IC process for applications requiring up to 170 V collector to emitter breakdown from both NPN and PNP transistors. Examples of such applications are subscriber line interface circuits for telephone central offices, CRT driver applications, and high voltage audio amplifiers [45]–[48]. For such high voltage bipolar ICs, which necessarily have thick epitaxial layers, the dielectric isolation scheme used in VIP-4H has a large die size advantage over traditional junction isolation. An additional benefit is the elimination of all parasitic substrate devices, which improves latchup immunity and radiation hardness.

Process Architecture: The starting materials is 2.5 μm of $\langle 100 \rangle$—oriented SOI over a 1 μm buried oxide fabricated using a BESOI process obtained from commercial vendors. After implantation and annealing of n+ (antimony) and p+ (boron) buried layer, and an n-type (phosphorus) "sinker-up" (which goes in NPN collector contact regions, as well as forming the buried layer of low-voltage NPN transistors), a thick (>20 μm) high-resistivity n-type epitaxial layer is grown. P-well, n-sinker, and p-sinker regions are then defined and implanted through a screen oxide. Active and field areas are defined by a standard nonrecessed LOCOS oxidation. Incorporated into the field oxidation cycle is a high-temperature anneal for the sinkers and p-well. Plasma-enchaned tetraethylorthosilicate (TEOS) source was used as a trench hard-mask for the deep trench etching in a magnetically enhanced RIE system using $HBr : NF_3 : He$–O_2 chemistry. An isotropic etch and sacrificial oxidation were used to remove any damages created on the trench sidewall. After growth of a trench liner oxide, the trench was filled with polycrystalline silicon which was etched back and then oxidized to cap the trench surface.

The remaining process is similar to the VIP-3H process and formed the device extrinsic base and emitter regions. A cross sectional view of a complete deep trench isolated device is depicted in Fig. 8.

Electrical Results: Typical high-voltage transistor characteristics are also summarized in Table I. Output characteristics of mesh-emitter NPN and PNP transistors with approximately 1000 μm^2 emitter area are shown in Figs. 9 and 10. Note that the Early voltage V_a is very dependent on collector current. Most of

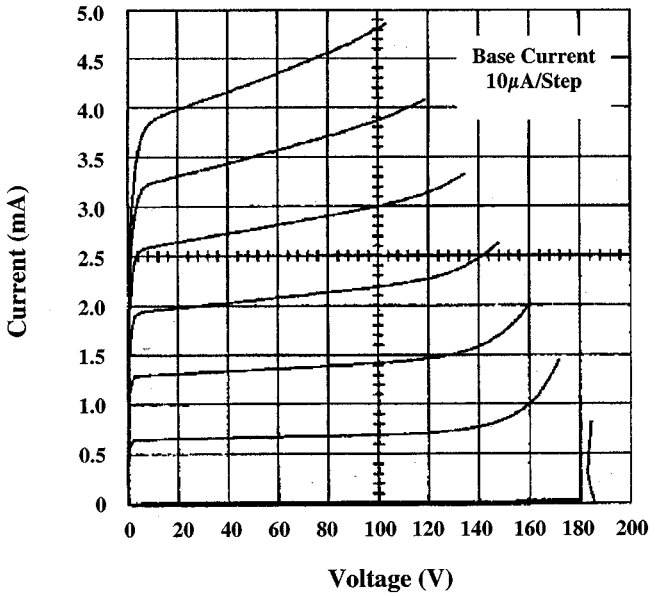

Fig. 9. I_c versus V_{ce} for a VIP-4H NPN devices.

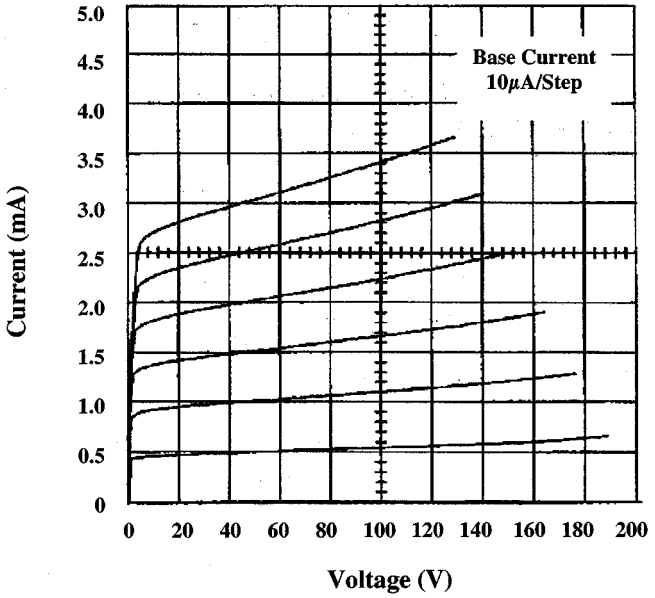

Fig. 10. I_c versus V_{ce} for VIP-4H PNP devices.

TABLE II
β AND Va FOR NPN/PNP DEVICES WITH AND WITHOUT GROWN INTERFACIAL OXIDE

	NPN		PNP	
	β	V_a	β	V_a
Wafer A	105	200	50	75
Wafer B	400	482	82	326

the observed increase in output conductance at high I_C is a result of self-heating [49], as the thermal conductivity of silicon dioxide is about a factor of 100 lower than that of silicon. The Early voltages given in Table I are measured at low current and voltage levels where self-heating effects are not significant. The isolation breakdown between adjacent trenches, as measured by a serpentine isolation test structures with 4.32 mm in length, was found to be 530 V with very low leakage.

IV. POLYCRYSTALLINE SILICON EMITTER AND INTERFACE CHARACTERIZATION

The current transport of the BJT, and the β and early voltage are a strong function of the monosilicon/polycrystalline silicon interface properties. The current gain is a ratio of the carriers injected from the emitter to base and the carriers backinjected from the base to the emitter. In the presence of an interfacial oxide, the tunneling-limited back injection of carriers decreases and the current gain increases. The theory for the transport has been investigated by many groups extensively [50], [51]. An experiment was performed to examine the effect of an interfacial oxide on NPN and PNP devices on the same wafer and is described below [52].

Experiments and Results: After device isolation formation in the VIP process, intrinsic bases were implanted in the device regions. HF-last clean was used on two sets of wafers. Wafer set A was loaded at 400 °C in the deposition tube and polycrystalline silicon was deposited at 625 °C as per the standard process. Wafer set B was loaded at 625 °C in air, heated at 625 °C for 20 min, and then polycrystalline silicon was deposited at 625 °C. Wafers were then rapid thermal annealed at 1060 °C for 20 s, and the standard process was continued. High-resolution TEM of the NPN and PNP emitter regions in wafer set A showed no interfacial oxide. In fact, epitaxial regrowth of the polycrystalline silicon emitter to the silicon substrate was observed as expected. High-resolution TEM in the PNP device of wafer set B showed a 22 Å oxide, while the NPN exhibited a 14 Å oxide. Table II shows the key electrical parameters of the wafer A and B. Figs. 11 and 12 show the SRP of the NPN and PNP devices without (wafer A-standard process) and with interfacial oxide (wafer B). It is clear that an oxide is present which prevents diffusion of emitter dopant in both types of devices in wafer B. The reduction in emitter diffusion due to the interfacial oxide results in a higher base peak doping and a higher base dose which increases the early voltage. Even though the effective base doping concentration is higher, the current gain is also significantly higher, which is due to the reduction

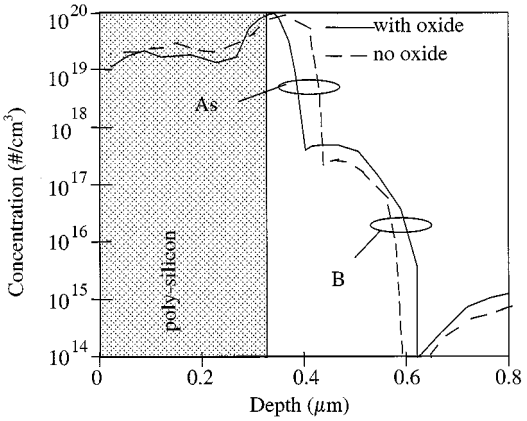

Fig. 11. SRP of the NPN with and without the grown interfacial oxide.

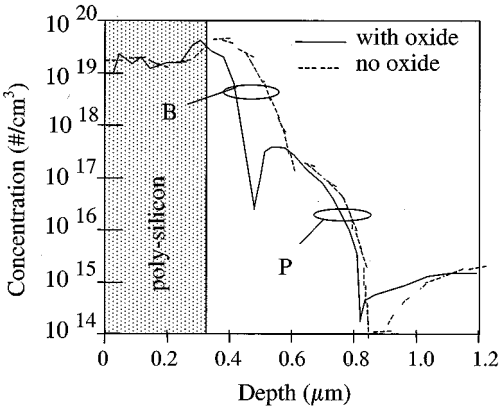

Fig. 12. SRP of the PNP with and without the grown interfacial oxide.

in the backinjected current. The enhancement in the PNP current gain of wafer B is less than the enhancement in the NPN current gain, as shown in Table II, due to two main reasons. Firstly, the probability for the back injected electrons is high and the barrier height is low, even though the interfacial oxide is thicker in the PNP. This does not increase the emitter injection efficiency as much. Secondly, the emitter is deeper for the PNP, which could cause increased recombination resulting in reduced enhancement. It should also be noted that the emitter resistance, not discussed in this paper, would also be increased due to the presence of the interfacial oxide. Earlier study extracted the probabilities of the backinjected electrons and holes and found the electron probability to be about 5× that of the hole back injection probability [52].

V. TRENCH ISOLATION AND CHARACTERIZATION

For high voltage devices, the lateral and vertical isolation of the devices from each other consumes significant space due to the distances required by depletion regions from adjacent devices. Deep trench isolation combined with BEBSOI wafers produces significant reduction in device size and the corresponding die size for high voltage processes when compared to junction isolation. In addition, the buried oxide layer provides additional reduction in space for vertical PNP devices since no N well diffusion is needed for the vertical PNP isolation. The field oxide isolation in high voltage devices is usually based on

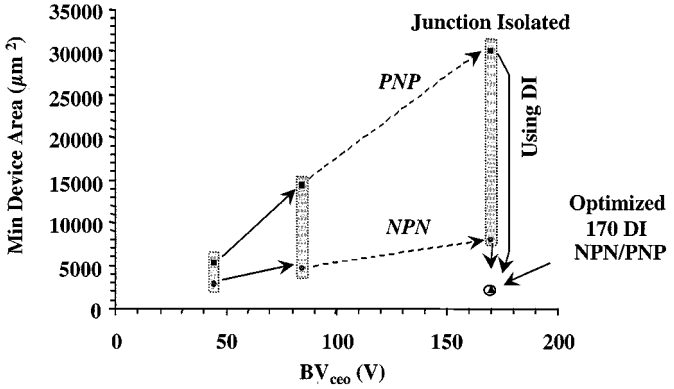

Fig. 13. Transistor size of minimum emitter (2 μm $\times$ 4 μm) from the VIP-3, VIP-3H, and VIP-4H technologies. Note the dramatic reduction in device size of the dielectrically isolated VIP-4H transistors when compared to its junction isolated counterpart.

LOCOS (or a derivative thereof) since replacement of the field oxide with a shallow trench isolation scheme will not provide a significant reduction in device size. Fig. 13 shows the total device size (including isolation) for the transistors from the three VIP technologies. For junction isolation (JI) technologies, the NPN device size is usually smaller than the PNP due to the additional area taken up by the N well isolation and its contact. However, it should be noted that when dielectric isolation (DI) is used, the device areas is reduced significantly.

For the VIP-4H process, a magnetically enhanced reactive ion etch system (MERIE) was used to define the deep trenches utilizing an $HBr/NF_3/He–O_2$ plasma chemistry [31], [35], [36], [55], [56]. The primary benefit of an azimuthally rotating magnetic field parallel to the wafer surface is enhancement of ionization rate by induction of electrons into helical trajectories between collisions allowing lower pressure operation without loss of etch rate [57]. Polycrystalline silicon is an ideal fill material since the mean free path is very long at typical low-pressure deposition conditions and can fill very high aspect ratio trenches. Oxide, on the other hand, can only be used to fill shallower trenches (less than 10 μm) and even then the fill shows voids when filled with thermal decomposition of TEOS at atmospheric pressure [31]. Subatmospheric pressure TEOS oxide has the potential to fill deep silicon trenches for reduced sidewall parasitic capacitance. Fig. 14 shows a TEM of the optimized and planarized deep trench isolation process used in the VIP-4H technology.

VI. Circuit Examples

A high-performance PNP in the signal path offers the opportunity for designing push–pull circuits for analog applications. In addition, a vertical PNP makes a truly precision band gap reference (where parasitic bipolar devices fail). The VIP technologies have been used to realize many voltage and current feedback amplifier circuits. A high-speed, low-power voltage-feedback operational amplifier was designed and demonstrated [58]. The low current version of this chip has a bias current of 2.5 mA at $\pm$15 V supply and a bandwidth of 110 MHz. The slew rate was 2000 V/μs. Another version of the circuit exhibited a bias current of 6.5 mA at the same supply voltage and a bandwidth of 200 MHz [59]. These circuits were also shrunk to produce

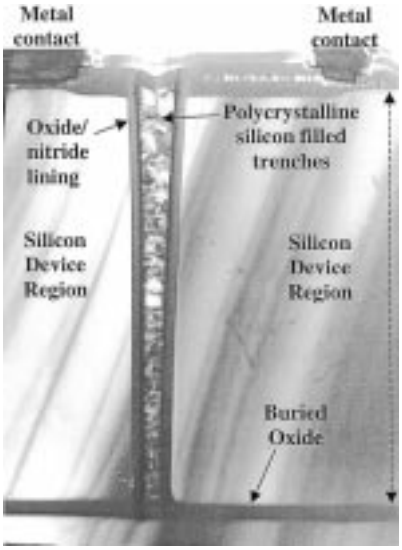

Fig. 14. Cross-sectional TEM of the deep trench isolation structure isolating two adjacent thick SOI device regions in the VIP-4H process.

a high-speed, voltage-feedback operational amplifier capable of operating from $\pm$1.8 V to $\pm$20 V supplies and driving infinite capacitive load. Silicon evaluations showed 188 MHz bandwidth and 1500 V/μs slew rate. The die size was 38 $\times$ 46 mil^2 in a tiny SOT package [60].

Another application of the high voltage process is in the cathode ray tube (CRT) which requires high-voltage and high-speed drivers (in excess of 40 MHz). Usually, discrete components are used to realize CRT Display drivers due to the lack of high-frequency and high-voltage monolithic approaches. A cascode output driver stage is used to allow for output voltage swings in excess of the BV_{ceo} (but not BV_{ces}) of the devices. In the VIP-3H technology, a family of monolithic CRT Drivers has been designed which is capable of achieving a 40 V p-p swing in less than 9.5 ns into 12 pF loads [62]. The use of vertically integrated high voltage PNP transistors not only simplifies circuit design, but improves performance. The output stage is an example of a high power, high frequency stage that is difficult to implement in a process with only high frequency NPN transistors. The close performance characteristics of the two device polarities allow high speed symmetrical drive to the CRT cathode.

VII. Conclusions

Complementary bipolar technologies are a cornerstone of analog circuits such as voltage and current feedback amplifiers, high-precision current mirrors, and push–pull circuits. This paper presented a detailed background and description of silicon complementary bipolar process technologies. Specifically, a family of processes called VIP™ was described with technology versions at 40, 85, and 170 V device breakdowns. The 40 and 85 V processes were junction isolated but the 170 V process was dielectrically isolated with deep trenches and SOI wafers. Key process issues such as the polycrystalline silicon emitter optimization and trench isolation were discussed. Circuit examples were provided to demonstrate the viability and usefulness of the technologies.

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