Silicon-on-insulator processes for the fabrication of novel nanostructures

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In this brief report, we discuss novel single crystal structures for electronic device and microelectromechanical system applications using processes that employ selective epitaxial growth (SEG) and silicon-on-insulator (SOI) wafers. Selective epitaxial growth of silicon is used to provide robust, reliable mechanical and electrical contacts between the SOI layer and the substrate. Subsequent removal of the buried oxide results in single crystal structures suspended in air. The films can then be thinned using wet or dry etching or thinned using sacrificial oxidation steps with the possibility of forming ultrathin SOI layers. Diodes formed at the substrate–SEG junction demonstrate high breakdowns and low leakage indicating good electrical isolation between the SOI layer and the substrate. The silicon on air regions can be used for dual-gate metal–oxide–semiconductor devices, quantum wires, cantilevers, as a substrate for lattice mismatched epitaxy, ultrathin SOIs, and lateral field emission tips.
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I. INTRODUCTION

Silicon-on-insulator (SOI) technology has found increasing use in microscale applications in recent years. These applications include electronic and microelectromechanical system (MEMS) devices where single crystal silicon can offer the advantages of control and reliable electronic and mechanical properties. Silicon-on-insulator metal–oxide–semiconductor field effect transistors (MOSFETs) with single top gates are currently being used in commercial applications, while double gate (a gate on the top and bottom of channels) MOSFETs are projected to replace conventional bulk complementary MOS (CMOS) technology below the 30 nm gate length.[1,2] These novel devices, having low parasitic and high performance, need techniques by which to form ultrathin silicon layers as the device channel regions.[3,4] In addition, many new micromechanical applications that use microscale sensors and actuators are being proposed that use surface micromachined single crystal silicon.[5,6] Thin silicon cantilevers increase the sensitivity of detection while allowing possible piezo-resistive deflection detection schemes. Thus, there is a need to develop processes with which to form ultrathin SOI films for a wide variety of applications.

In this brief report, we discuss the use of bonded and etched-back SOI (BESOI) and selective epitaxial growth (SEG) to form ultrathin SOI layers. The process uses a novel anchoring scheme using SEG of silicon to suspend the structures above the substrate. Initial experimental results are presented that demonstrate the viability of such a process. The process can be applied to a wide variety of applications such as double gate MOSFETs, compliant substrates for lattice-mismatched epitaxy, thin cantilevers and diaphragms for micromechanical applications, sub-100 Å silicon wires, and lateral field emission and scanning probes.

II. PROCESS FLOW

The fabrication process begins with a commercially available bonded and etched-back silicon-on-insulator wafer, which had a 2.5 μm, *N*-type SOI layer, a 1.0 μm buried oxide, and a *P*-type substrate. A 0.23 μm oxide was then grown in wet ambient on the SOI layer. A $CHF_3:O_2$ (18:1) reactive ion etch was used at 270 W to etch through the oxide/SOI/buried oxide stack, using a photoresist layer as the mask. A cross section of this step is shown in Fig. 1(a). The reactive ion etch damage was annealed at 950 °C for 15 min in N_2. A hydrogen prebake step at 970 °C in a Gemini I pancake-type reactor was used to etch any native oxide from the substrates and the sidewall of the SOI. Then, selective epitaxial growth of silicon was performed in the same reactor at $T=970$ °C and $P=40$ Torr using hydrogen as the carrier gas, dichlorosilane (DCS) as the source, and HCl to maintain selectivity over the oxide. The SiH_2Cl_2 flow rate was 0.22 slm, the HCl flow rate was 0.66 slm, and the hydrogen flow rate was 60 slm and the resulting growth rates were about 0.12 μm/min. The *N*-type silicon crystal, with doping of about $4e15$ atoms/cm^3, was grown vertically from the substrate and laterally from the sidewall of the SOI layer until the growth fronts merged and grew out at the top of the seed-hole regions to a total thickness of about 4 μm, as shown in Fig. 1(b). Hence, the SEG regions provided an anchor between the SOI layer and the substrate. At this step, a chemical mechanical polishing step can be used to remove excess overgrowth and to planarize the silicon if needed.

Next, the top of the overgrown silicon regions was oxidized and a photoresist mask was used to define a dog bone-shaped device active region encompassing the anchor regions and an SOI region in between the anchors. The top oxide was wet etched and the underlying SOI layer was also removed by either a reactive ion etch or hot potassium hy-

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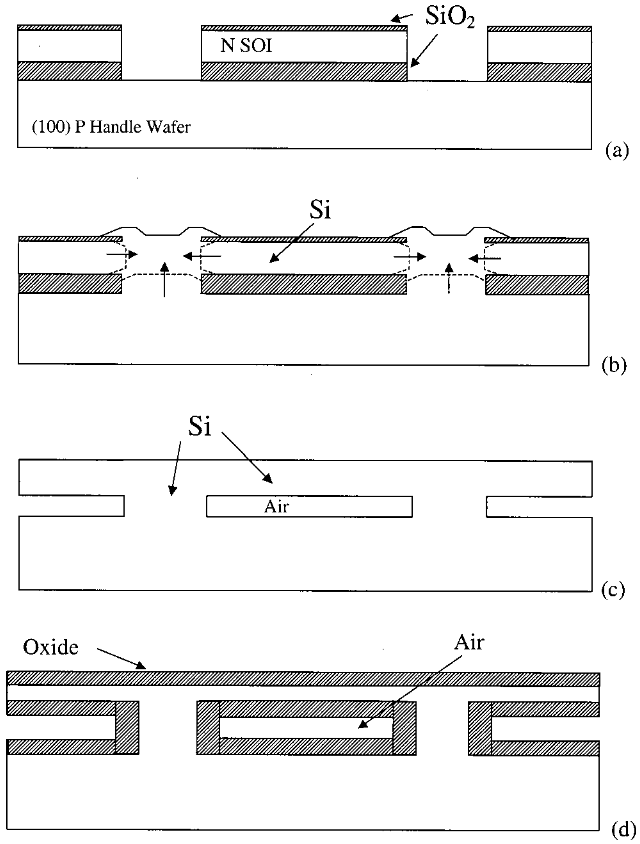

FIG. 1. Cross section of process flow for ultrathin SOI in air fabrication.

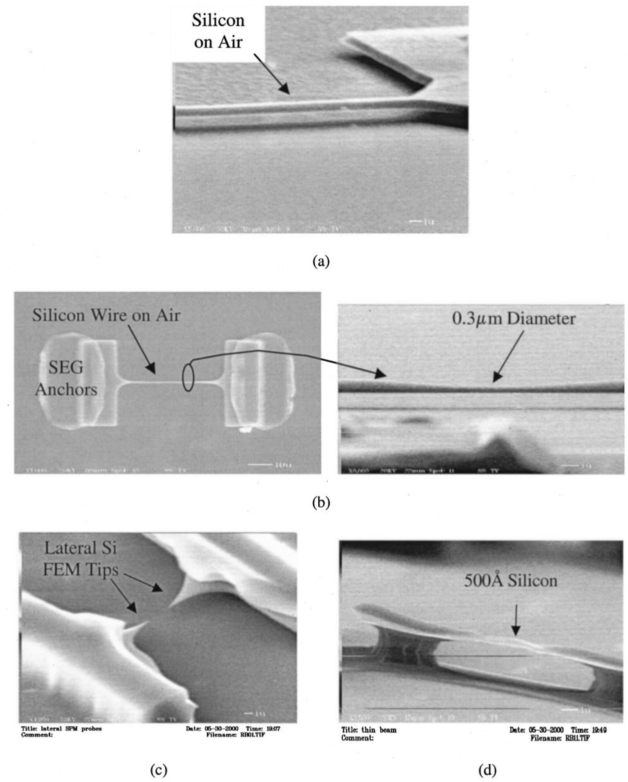

FIG. 2. Scanning electron micrographs showing the single crystal structures suspended in air with SEG anchors.

droxide, stopping at the buried oxide layer. Next, the wafers were placed in HF solution to completely etch off all oxide and to release the silicon membranes, diaphragms, wires, cantilevers, etc. defined by the earlier mask. The cross section at this point is shown in Fig. 1(c). The silicon-on-air film thickness, at this point, is hence defined by the initial SOI thickness. However, the thickness can be reduced by the following possible means: (i) wet silicon etching in mixtures of HF, HNO_3, etc., (ii) dry etching in XeF_2,[7] (iii) selective chemical vapor phase etching (SCVE) of silicon in HCl at 850–1000 °C,[8,9] or (iv) oxidation and subsequent etching of the oxide to thin the membranes. Options (iii) and (iv) will most likely result in the best crystallographic surfaces of the film for further device processing, however, option (iv) does results in stress induced from the oxidation process occurring at both sides of the membranes.

III. EXPERIMENTAL RESULTS

The active area mask was used to define a dog bone-shaped structure shown in the scanning electron microscope (SEM) micrographs in Figs. 2(a) and 2(b), which show the structure after it has been released by removing all the oxide. The 2.5 μm thick SOI layer was initially thinned to about 1.1 μm by two successive oxidations which produced about a 7100 Å thick oxide on a bare wafer. The oxidations were performed at 1050 °C, higher than the oxide reflow temperature, so that thermal stress is minimized. Figure 2(b) shows a silicon wire formed by reducing the width (of the initial 1.1 μm thick silicon pattern) to 1 μm and then performing the oxidations such that an approximately 0.3 μm diam wire was formed. Such a structure also provides the possibility of thinning the silicon to a sub-50 Å range diameter by self-limiting oxidation processes, which are known to produce stress-induced retardation effects at temperatures below the oxide reflow temperature.[10] If the oxidation is performed at a higher temperature, all the silicon can be consumed at the point where silicon is thinnest. This scheme is shown in Fig. 2(c), where lateral silicon tips can form for field emission and lateral scanning probe applications. If the structure being released is a plate, then device regions like those shown in Fig. 2(d) can form where the silicon region is thin and be suspended in air through anchor points. These thin diaphragms can be used for complaint substrate applications for growth of lattice-mismatched substrates.

The process demonstrated in this report provides low thermal resistance contact while providing the electrical isolation needed for many transducer and electronic device applications. In addition, it also solves the problem of uncontrollable lateral etching of the buried oxide to release the silicon diaphragms when an anchor is not present, as in other MEMS SOI processes.[11] Growth of *N*-type silicon on P substrates forms a diode which is electrically characterized by making contact to the SOA layer and the back of the wafer, as shown in Fig. 3, along with the breakdown characteristics. The junction showed low leakage and breakdown of about 54 V at 10 μA, respectively, which correlated well with the calculated breakdown for such a function and is well above

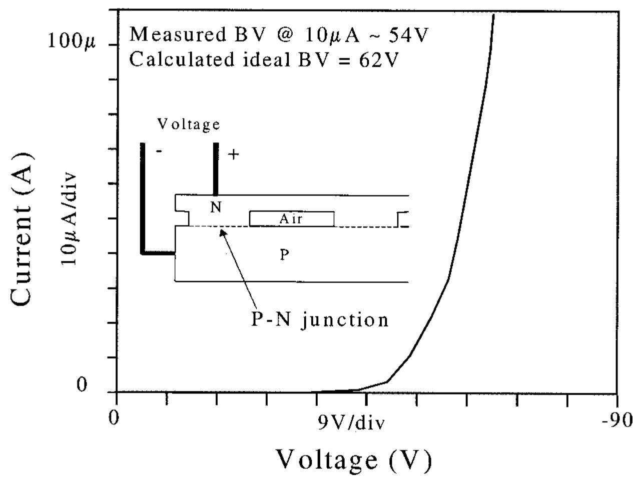

FIG. 3. Curernt vs voltage for the *p/n* isolation diode.

the pull-down voltages for typical gap thickness, if such structures were to be used for surface MEMS applications.[12]

IV. CONCLUSIONS

In this work, a novel process to form a SOI structure suspended in air was devised and the feasibility of such a process was demonstrated. The structure provides electrical isolation while providing good thermal contact to the substrate. The process has the potential to form many novel structures including very thin silicon layers (sub-200 Å) for use in advanced double gate MOS devices, for ultrasensitive MEMS based cantilevers and microactuators, quantum wires, and lateral field emission and scanning probes.

ACKNOWLEDGMENT

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