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Modeling and characterization of deep trench isolation structures

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Abstract

In this paper, we present a simple equivalent electrical circuit model and sidewall interface characterization results for a deep trench isolation structure. The trench structures used in the study consisted of n-silicon/undoped trench/n-silicon. The trenches were filled with undoped polycrystalline silicon and the trench sidewall was lined with thermal oxide and a deposited silicon nitride. The capacitance–voltage characteristics across the trench were measured and compared against the model predictions. The circuit model includes the effect of the space-charge region and recombination–generation currents in the undoped polycrystalline silicon trench fill material. The Terman method was used to extract the silicon/oxide sidewall interface density and the mid gap value was found to be less than 10^{-10} #/cm^2-eV. © 2001 Elsevier Science Ltd. All rights reserved.

Keywords: Trench isolation; High voltage isolation; Trench modeling; Trench sidewall interface

1. Introduction

In integrated microelectronics circuits, electrical isolation is needed between adjacent semiconductor devices. Typical isolation technique consists of a combination of junction isolation and local oxidation of silicon (LOCOS). More recently, however, LOCOS isolation is being replaced with a shallow trench isolation (STI) process for deep sub-micron CMOS processes. In the case of high voltage devices for analog and power applications, LOCOS isolation in combination with deep trench isolation has been used [1–4]. If high voltage devices were to be isolated with junction isolation, the inter-device separations would become too large and impractical. Thus, the use of deep trench isolation significantly reduces the device size and the die size, hence reducing the device cost.

Transistors separated by a deep trench structure, however, are capacitively coupled to each other and can affect the electrical characteristics of adjacent transistors. It is therefore important to understand and model the isolation structures as a function of voltage and frequency. The quality of the trench sidewall (i.e. the silicon/trench liner interface) is also very important in determining the reliability and leakage characteristics of the interface. Interface state density measurements can thus be used to evaluate the quality of this interface. The purpose of this paper is to report on the measurement results of capacitance–voltage behavior of silicon regions isolated with deep isolation trenches. A model is also presented and validated with measurements. The model takes into account the space-charge region and the recombination-generation mechanisms in the polycrystalline silicon in the trench. In addition, interface state density measurements are performed to evaluate the trench sidewall interface.

2. Experimental details

2.1. Process information

A novel deep trench isolation process for high voltage silicon on insulator (SOI) integrated circuits has been developed and reported in detail previously [4–6]. A cross-sectional TEM of such a trench is shown in Fig. 1. The staring material was a 25 μm thick SOI wafer. Oxide was patterned as a hardmask and trenches were etched using a magnetically enhanced reactive ion etching (MERIE) system (AMAT P5000).

The sidewall of the trenches were oxidized, coated with LPCVD silicon nitride, and then filled with undoped polycrystalline silicon, which was deposited using LPCVD from silane at 625°C. Subsequent processing details have been given elsewhere [4]. The depth of the trench, D, was 25 μm. The width of the trench (i.e. thickness of poly in the trench, t_{poly}), thickness of SiO_2, (t_{OX}), and thickness of Si_3N_4 (t_N) were 1, 0.45, and

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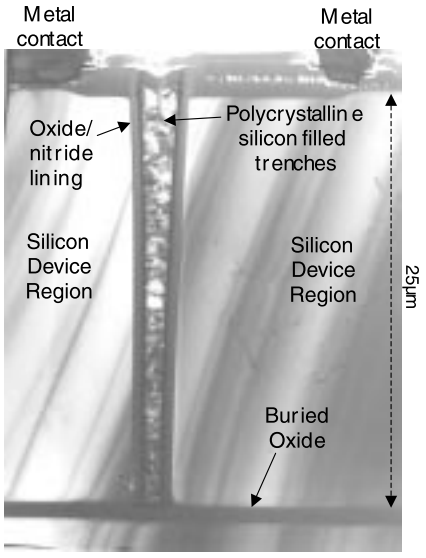

Fig. 1. A cross-sectional TEM of the deep trench isolation structure isolating two adjacent thick silicon on insulator (SOI) device regions.

0.3 μm, respectively. The concentration of the n-type silicon was 4.5×10^{14} #/cm^3 as determined by spreading resistance profiles of the SOI regions. A total width of 20 inter-digitated silicon device islands, Z, was 0.432 mm, resulting in a capacitor area of 25 μm × 0.432 mm.

2.2. Measurements and discussion

The capacitance–voltage measurements on the trench isolation structure were performed with an HP4274A LCR meter. Voltage was swept from −20 V to +20 V and then swept in the reverse direction. No change in the curves was observed indicating the absence of any mobile charges. The voltage was stepped at a rate of 0.02 V/s. To stabilize inversion capacitance, a delay time of 180 s was used before starting the sweep and a hold time of 60 s was used before repeating the sweep. Fig. 2 shows the measured variation in capacitance with voltage. The results are as expected of a SIS (silicon–insulator–silicon) structure. When a positive voltage is applied to the silicon island on the left side, for example, the silicon on the left side is depleted and the silicon on the right side is accumulated. As the positive voltage on the left island is increased, the left silicon/insulator interface eventually inverts and the capacitance decreases to a fixed value. When a negative voltage is applied to the island on the left side, the silicon on the left side is accumulated and the silicon on the right is depleted. As the negative voltage is increased, the right silicon/insulator interface eventually inverts. Hence, the capacitance–voltage curve is expected to be symmetric around $V = 0$. This is indeed the case as measured experimentally. As shown in Fig. 2, the capacitance was also measured as a function of frequency and the accumulation and inversion capacitances were found to increase with decreasing frequency.

3. Proposed model and verification

Since the capacitance of n-type silicon, oxide, and nitride

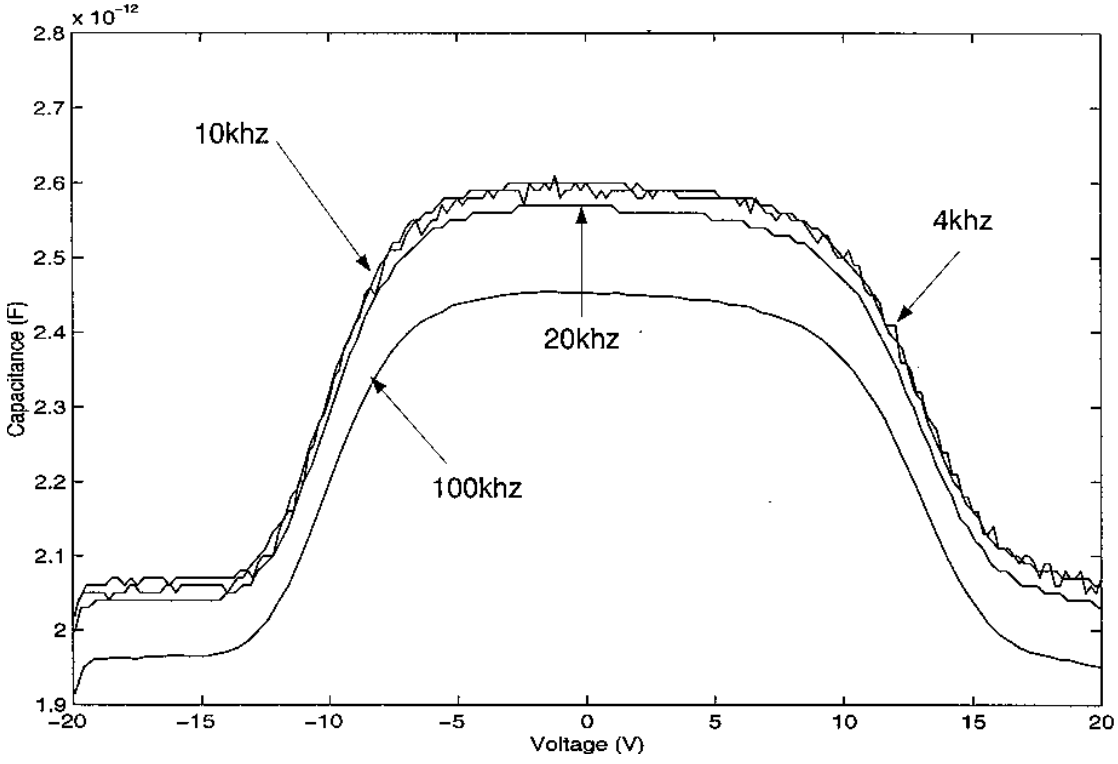

Fig. 2. Capacitance–voltage characteristics of the Si/trench/Si structure measured at different frequencies.

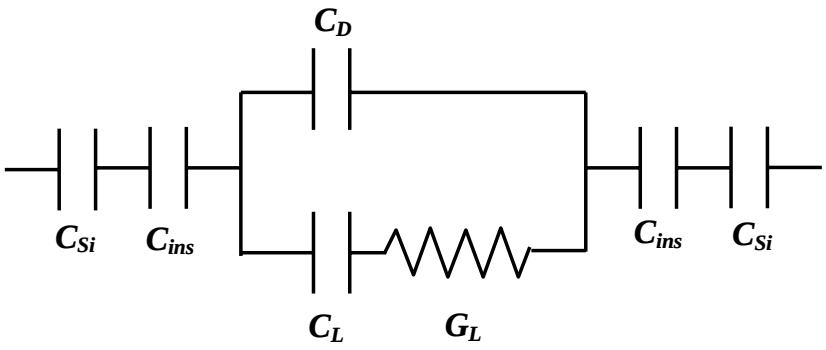

Fig. 3. A proposed model/equivalent circuit for the trench isolation structure.

are not a function of frequency for these test frequencies, the frequency dependent characteristics are determined by the undoped polycrystalline silicon trench fill material. Using this information and the data from the physical structure of the trench, we can propose a simple equivalent circuit for the trench isolation structure. The following assumptions are made while developing this model: (i) the parasitic capacitance from the bonded oxide and substrate is ignored; (ii) the polycrystalline silicon is assumed to be undoped; and (iii) the intrinsic carrier concentration is assumed to be around 10^{10} #/cm^3 in the polycrystalline silicon. Fig. 3 shows the proposed circuit model for the trench structure. The fixed capacitance due to the parallel combination of the oxide and the nitride film, C_{ins}, can be expressed as

$$C_{\text{ins}} = Z \times D/(t_{\text{OX}}/\varepsilon_{\text{SiO}_2} + t_{\text{N}}/\varepsilon_{\text{Si}_3\text{N}_4}) \tag{1}$$

The silicon region on either side of the trench can be modeled as a capacitance that is a function of voltage and is the same as an oxide/silicon interface capacitance. This capacitance is termed as C_{Si} and will be C_{inv} when either side of the structure is inverted (where W_{inv} is the maximum depletion length at inversion). Hence, in inversion region, $C_{\text{Si}} = C_{\text{inv}}$ as given below:

$$C_{\text{inv}} = \varepsilon_{\text{Si}} \times Z \times D/W_{\text{inv}} \tag{2}$$

Since the polycrystalline silicon layer is undoped, a depletion layer will exist in the polycrystalline silicon layer for the whole voltage range and hence it can be modeled as a depletion capacitance, C_{D}, given by

$$C_{\text{D}} = \varepsilon_{\text{poly}} \times Z \times D/t_{\text{poly}} \tag{3}$$

In addition, recombination and generation processes will also occur within the polycrystalline silicon. These R–G processes will result in charge perturbations within the polycrystalline silicon layer when an ac signal is applied across the trench. These charge perturbations can be modeled as a capacitance and resistance, C_{L} and G_{L} of the polycrystalline silicon layer. This proposed model is consistent with earlier reports [7,8].

The components of the model representing the trench polycrystalline silicon itself are actually a function of frequency. At high frequencies, the impedance of C_{D} will dominate and the ac current will flow through it. Hence, C_{L} and G_{L} can be neglected and the equivalent network for the trench can be simplified accordingly. The equations of total accumulation and inversion capacitance for the whole structure at high frequencies can then be calculated as follows:

$$C_{\text{acc-total-HF}} = \frac{C_{\text{ins}} C_{\text{D}}}{2C_{\text{D}} + C_{\text{ins}}} \tag{4}$$

$$C_{\text{inv-total-HF}} = \frac{C_{\text{acc-total}} C_{\text{inv}}}{C_{\text{acc-total}} + C_{\text{inv}}} \tag{5}$$

At lower frequencies, a part of the current will flow through the recombination–generation components, C_{L} and G_{L}. G_{L} is determined by the resistivity of undoped polycrystalline silicon, and is given by

$$G_{\text{L}} = \left[\frac{\rho_{\text{poly}} \times t_{\text{poly}}}{(Z \times D)} \right]^{-1} \tag{6}$$

The capacitance due to recombination–generation processes, C_{L}, can be related to the trap density in the undoped polycrystalline silicon. Hence, a relationship between capacitance and trap density must be derived. The charge density in the polycrystalline silicon layer can be written as $n_{\text{t}}(\phi) = N_{\text{t}}\phi$ where N_{t} is the bulk trap state density and ϕ is the potential. Then, ρ_{L} and C_{L} can be expressed as follows:

$$\rho_{\text{L}}(\phi) = -qn_{\text{t}}(\phi) \tag{7}$$

$$C_{\text{L}} = \frac{\varepsilon_{\text{poly}} \rho_{\text{L}}(\phi_{\text{ss}})}{\left[-2\varepsilon_{\text{poly}} \int_0^{\phi} \rho_{\text{L}}(\phi)\, \mathrm{d}\phi \right]^{1/2}} \tag{8}$$

where ϕ_{s} is the surface potential at a certain gate voltage and ρ_{L} is the bulk charge density. Using Eqs. (1)–(3), (6) and (8), equations for the low frequency total accumulation and inversion capacitance can be derived as follows:

$$C_{\text{acc-total-LF}} = \frac{2\text{Gp}^2 C_{\text{ins}} + \omega^2 \text{Cp} C_{\text{ins}}(2\text{Cp} + C_{\text{ins}})}{4\text{Gp}^2 + \omega^2(2\text{Cp} + C_{\text{ins}})^2} \tag{9}$$

Table 1
The calculated and measured values for the inversion and accumulation capacitance

	100 kHz		20 kHz		10 kHz		4 kHz	
	Meas	Cal	Meas	Cal	Meas	Cal	Meas	Cal
Inversion capacitance (pF) @ 15 V	1.965	1.901	2.066	2.021	2.015	2.021	2.016	2.0225
Accumulation capacitance (pF) @ 0 V	2.449	2.415	2.564	2.616	2.592	2.616	2.581	2.616

$$C_{\text{inv-total-LF}} = \frac{G_{\text{acc}}^2 C_{\text{inv}} + \omega^2 C_{\text{acc}} C_{\text{inv}}(C_{\text{acc}} + C_{\text{inv}})}{G_{\text{acc}}^2 + \omega^2 (C_{\text{acc}} + C_{\text{inv}})} \quad (10)$$

where Gp and Cp is the equivalent capacitance and conductance including C_D, C_L, and G_L.

The above model was verified using calculations of the inversion and accumulation capacitance. It was assumed that there is no charge in the surface between the SiO_2 and Si_3N_4. A value of 1 MΩ cm was used for the resistivity of undoped polycrystalline silicon [9]. Eqs. (4) and (5) were used to calculate the inversion and accumulation capacitance at high frequencies and the results are shown in Table 1. As can be noted, using the structural dimensions and the above listed parameters, the accumulation and inversion capacitance values were well within 5% of the measured values. For the lower frequency regimes, N_t is really the only unknown and was used as a parameter to fit the measured inversion and accumulation capacitance values at these low frequencies. The best N_t fit value was found to be 2.69×10^{14} #/cm^3. This value of bulk trap density is lower when compared to published values in polycrystalline silicon [9] but could be attributed to the large grains in the film as observed in TEM. Even though the polycrystalline film was deposited at 625°C, subsequent heat cycles in the process must have recrystallized the film further and hence reduced the bulk trap density. As shown in Table 1, the measured and calculated values of accumulation and inversion capacitances at 4, 10, and 20 kHz are again very close, indicating the validity of the model.

4. Interface state density extraction

The interface state density at the silicon/oxide trench sidewall is another important parameter which can give an indication of the quality of the trench etch and the trench lining process. An inferior sidewall quality can result in unwanted parasitic leakage currents along the trench sidewall and long-term reliability issues. In the given structure, it is difficult to measure the interface state density due to the trap density in the polycrystalline silicon in the trench and its effect on the CV curves at low frequencies. Hence, the high frequency regime is used where the accumulation capacitance is not varying with frequency and the polycrystalline silicon can be treated as an insulator. The interface state density was extracted using the Terman method [10], which can be used to extract Dit as low as

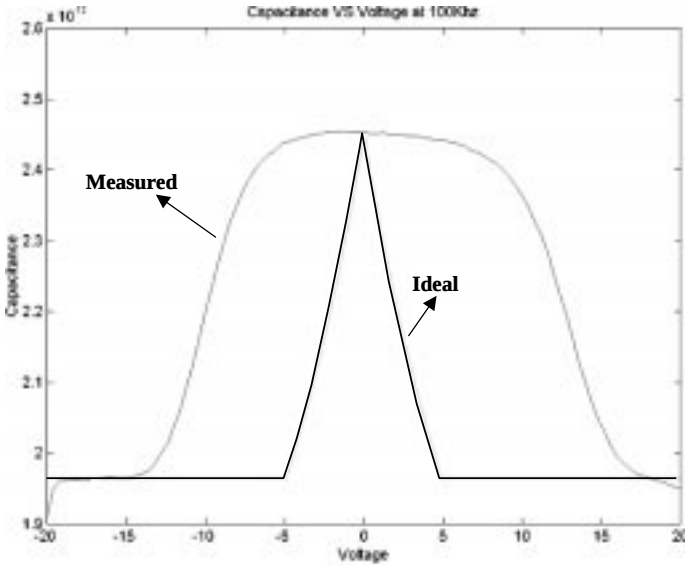

Fig. 4. The measured and ideal (calculated) capacitance–voltage curve at 100 kHz.

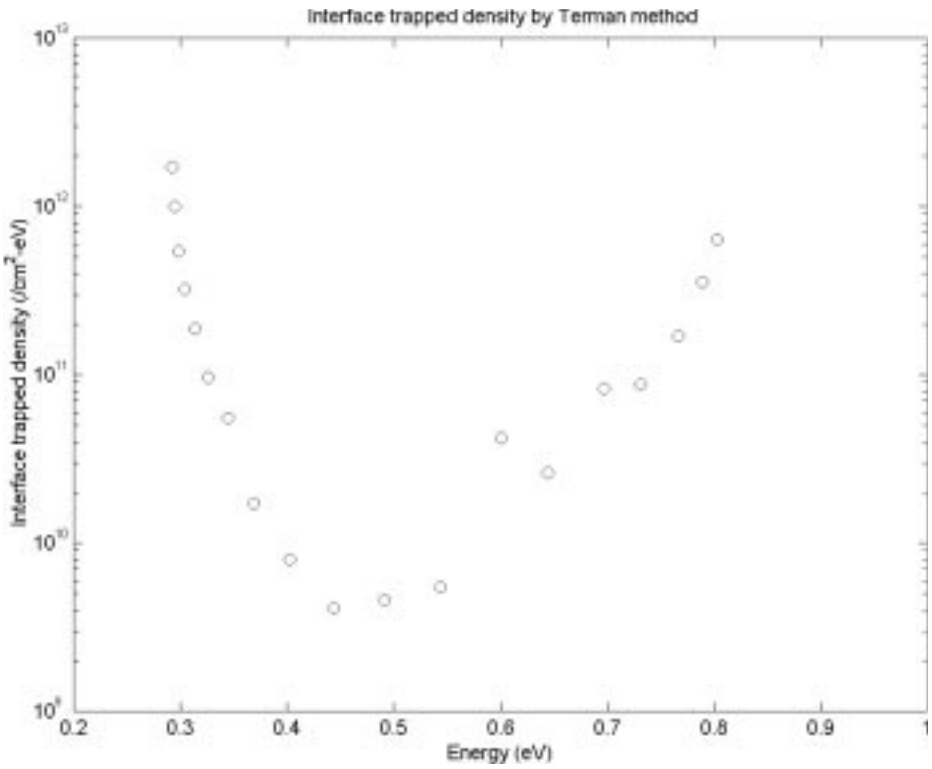

Fig. 5. Interface state density in the band gap extracted using Terman's method.

10^9 #/cm^2-eV provided that the capacitance is measured with a precision of 0.001–0.002 pF (which was possible with our apparatus). Given the known physical parameters, the ideal delta depletion approximated CV curve can be calculated and the data are shown in Fig. 4. The difference in ideal and the actual CV curve in the depletion region can be used to extract the interface state density as per the Terman method. The ideal gate voltage is given by

$$V_{\text{Gideal}} = \phi_{\text{S}} + V_{\text{ins}} \tag{11}$$

where ϕ_s is the surface potential and V_{ins} is the voltage across the insulator given by

$$V_{\text{ins}} = qN_{\text{D}}W_{\text{dep}}\left(\frac{2t_{\text{ox}}}{\varepsilon_{\text{ox}}} + \frac{2t_{\text{N}}}{\varepsilon_{\text{N}}} + \frac{t_{\text{undopedPoly}}}{\varepsilon_{\text{undopedPoly}}}\right) \tag{12}$$

The above equation has been modified for the particular trench structure under study. The interface state density then can be obtained from the ϕ_s–gate voltage relationship as follows [10]:

$$D_{\text{it}} = \frac{C_{\text{acc}}}{q}\frac{\text{d}(V_{\text{Gmeasured}} - V_{\text{Gideal}})}{\text{d}\phi_{\text{s}}} \tag{13}$$

Fig. 5 shows the interface state density that drops to below 10^{10} #/cm^2-eV at mid-gap. This value is very low and could possibly be due to the fact that during the processing of the trench module, special effort was taken to eliminate any sidewall damage. After the reactive ion etching of the trench, an isotropic etch was used to remove the sidewall material. Subsequently, a sacrificial oxidation step was used, in addition to the growth of the 0.45 μm thick sidewall thermal oxide in an HCl ambient. Even though the limitations of the Terman method have been pointed out in detail in the past [11], in our study it does give a strong evidence of a good quality sidewall at the trench oxide/silicon interface under the given processing conditions.

5. Conclusions

In this paper, we experimentally characterized the trench isolation structures using capacitance–voltage measurements. A model was presented which took into account the capacitance at the silicon/insulator interface, the insulator capacitance, the polycrystalline silicon trench fill depletion capacitance and the capacitance and conductance in the polycrystalline silicon due to recombination–generation. The model fitted well with experimental measurements at 100 kHz if the polycrystalline silicon R–G capacitance and conductance was ignored. The model also fitted well with experimental measurements for lower frequencies taking into account the conductance of the undoped polycrystalline silicon and the polycrystalline silicon bulk trap induced capacitance. The calculated values of accumulation and

inversion capacitance using the model were within 5% of the measured result. The Terman method was used to extract the silicon/oxide sidewall interface density and the mid-gap value was found to be less than 10^{-10} #/ cm^2-eV.

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