Precision Electrical Trimming of Very Low TCR Poly-SiGe Resistors

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***Abstract*—Precision electrical trimming of stacked Si/SiGe polycrystalline resistors available from the extrinsic base structure of a SiGe BiCMOS technology has been demonstrated for the first time. It is shown that pulse current trimming techniques can be used to trim the poly-SiGe resistors by up to 50% from their original values with accuracy better than ±0.5%. The temperature coefficient of resistance (TCR) is shown to be linearly proportional to the percent change in electrically trimmed poly-SiGe resistance. Finally, we demonstrate resistance cycling using an electrical trim/recovery sequence, indicating that the technique is reversible and is governed by dopant segregation/diffusion mechanisms. The results are consistent with those obtained on conventional polysilicon resistors suggesting that the introduction of a strained SiGe layer does not adversely affect the electrical trim properties of these resistors.**

***Index Terms*—Adjustable resistance, electrical trim, electrically trimmable, GeSi, high-precision resistors, poly-SiGe, polycrystalline Si/SiGe thin-films, polysilicon, resistance recovery, resistor trim, resistors, SiGe, TCR, temperature coefficient of resistance, tunable resistors.**

I. Introduction

MANY high-speed mixed-signal IC applications, (such as low offset voltage operational amplifiers, precision voltage reference circuits, analog frequency tuning circuits, VCO's D/A and A/D converters) require high performance technologies that are ultimately limited by the accuracy of both active and passive components of the technology. Recently SiGe BiCMOS has emerged as a viable technology for RF single chip solutions in wireless communication products [1]. However, inaccuracies and variations in thin film and thick film resistor deposition typically result in 10% to 20% variation from the designed resistor values [2] while best case poly-SiGe resistance variations have been reported at 7.2% [3]. Clearly there is a need for methods which can precision trim poly-SiGe resistors with ±0.5% or better accuracy while having minimum impact on die size requirements, fabrication, test, and chip cost. One of the more promising techniques to achieve this is electrical trimming of heavily doped polysilicon resistors [4]–[8]. In this letter, we demonstrate for the first time that poly-SiGe resistors available from the standard extrinsic base process of a SiGe BiCMOS technology can be electrically trimmed with better than ±0.5% precision in the range of 0% to 50% trim from their original values. We also investigate the effects of electrical trim on the temperature-coefficient-of-resistance (TCR) and show that the trimming is reversible.

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II. Experiment

Poly-SiGe resistors, fabricated using a standard SiGe BiCMOS process [9], were investigated for use in precision trim IC applications. A commercially available RPCVD reactor was used to grow the Si/SiGe stack in the HBT process as described by Bashir *et al.* [10]. RPCVD growth on a 0.4 μm LOCOS field oxide results in a polycrystalline Si/SiGe film (used for resistor formation) while simultaneous growth on active silicon regions results in the epitaxial SiGe HBT base formation with 10% peak quasitriangular Ge profile.

Resistance measurements were made on wafer using Kelvin test structures with a HP 4156B Precision Semiconductor Parameter Analyzer and a low-leakage Cascade wafer probe station with temperature control capability ranging from -65 °C to $+200$ °C. In order to assure accuracy of the measurement system, a reference resistor was chosen and monitored both before and after each experiment. Accuracy of the system was better than ±0.02% for a 1.0 kΩ resistor. The polysilicon resistors were trimmed by both pulse-current trim techniques [6] and by current sweeps to the trim target resistance value.

III. Results

A typical resistance characteristic versus cumulative trim current pulse density is shown in Fig. 1 for a single 1.9 kΩ poly-Si/SiGe resistor with boron doping of 6×10^{19} cm^{-3}.

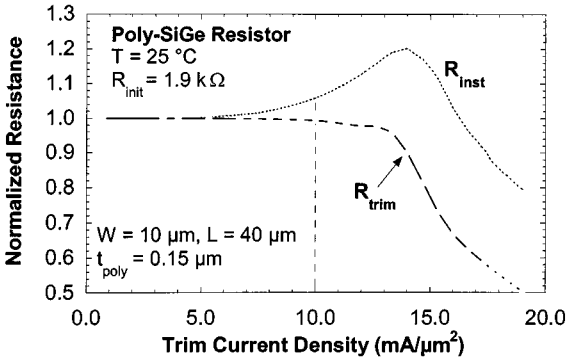

Fig. 1. Typical normalized resistance versus trim current density characteristic. Solid line shows the trim resistance values (R_{trim}) measured at a (low) current density of 160 μA/μm^2 after applying the trim current density indicated on the horizontal axis to the resistor. The dashed line shows the instantaneous resistance measured during the applied trim current-pulse (2.0-s pulse width).

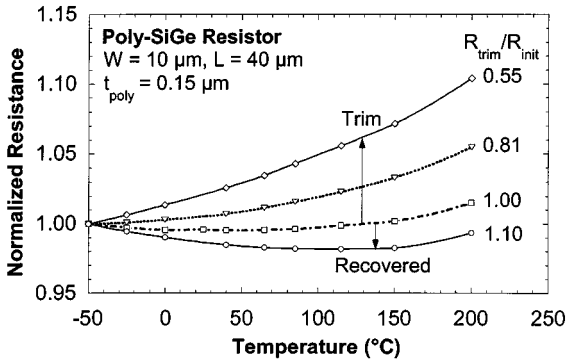

Fig. 2. Normalized poly-SiGe resistance measured at 160 μA/μm^2 versus temperature for both trimmed and recovered resistors, where the resistance has been normalized to the resistance measured at -50 °C.

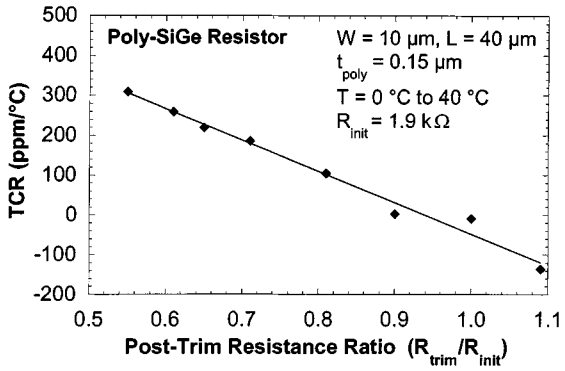

Fig. 3. Temperature coefficient of resistance (TCR) measured between 0 °C and 40 °C at a current density of 160 μA/μm^2 versus the ratio of post-trim resistance (R_{trim}) to pre-trim resistance (R_{init}). Note: Ratio values greater than 1.0 are obtained by recovery techniques.

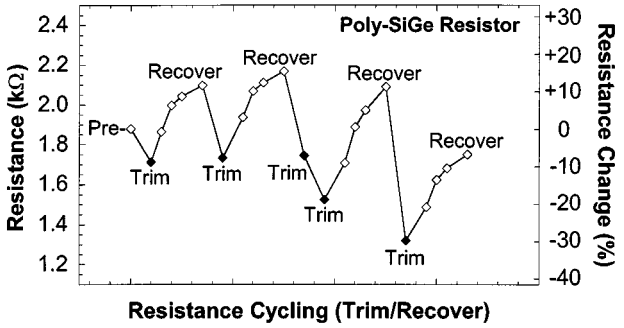

Fig. 4. Poly-SiGe resistance cycling showing both resistance trimming and resistance recovery (units on the horizontal axis are arbitrary). The trim/recovery sequence consisted of first trimming the resistor with a 4.0-s current sweep to 14.0 mA/μm^2. The resistor was then recovered by applying a recovery current of 11.7 mA/μm^2 for a total time of 40 000 s. The process was repeated several times and included trimming the resistor to different values.

Each point on the solid curve represents the normalized resistance measured at a current density of 160 μA/μm^2 after having applied a succession of trimming current pulses with increasing amplitude. The dashed line, which represents the normalized instantaneous resistance measured during the application of a trim current pulse, initially shows an increase in resistance due to Joule heating effects. An inflection point occurs at the onset of resistance trimming, followed by a roll-off in instantaneous resistance measured at higher currents where significant trimming has occurred in the resistor. From Fig. 1, several observations can be made. First, the initial polysilicon resistance is stable until a threshold current density is reached ($J_T \sim 10.0$ mA/μm^2). Second, when the trim current is increased above the trim threshold current the polysilicon resistance begins to decrease. Similar to heavily doped polysilicon [4]–[7], the poly-SiGe resistance change is permanent as long as the operating current density remains below the threshold trim current density. Third, the maximum shift in resistance is limited to approximately 50% by destructive open-circuit failure of the poly-SiGe film, caused by thermal vaporization of the film.

Another key parameter of interest for designers using poly resistors is the shift in resistance with temperature and how this is affected by trimming. With regard to the thermal variations, Fig. 2 shows the poly-SiGe resistance characteristic versus temperature, normalized to the value measured at -50 °C, for both trimmed and recovered resistors. These data show that the trimming of a resistor will cause its thermal characteristics to change. Also, it is clear that the TCR is not constant throughout the temperature range. With regard to the effects of trimming, Fig. 3 shows the room temperature (25 °C) TCR values measured for several poly-SiGe resistors versus the relative amount of trimming. The results in Fig. 3 clearly show a linear relationship of the TCR with respect to the trimmed resistance ratio. These results are consistent with those found in conventional polysilicon resistors, which indicate that electrical trimming of the poly-SiGe resistors is due to a reduction of the resistance at the grain boundaries [11]. It is also noted that the change in TCR remains within $\pm$200 ppm/°C for trim conditions ranging from $+10\%$ to -50% compared with those reported by other authors [6], [13] which can vary by more than 1000 ppm/°C in this trim range. This indicates that the very low TCR poly-SiGe resistors (as opposed to conventional gate polysilicon resistors) are more suitable for precision trim circuits that need to maintain their target value over a wide operating temperature range.

In agreement with results obtained on polysilicon resistors [6], [11], [12], [14], the change in resistance induced by elec-

trical trimming was found to be reversible by applying a recovery current pulse that is less than the final trim current pulse but greater than $J_T \sim 10.0$ mA/μm^2. Fig. 4 shows the ability to cycle the resistance by applying a sequence of resistance trim/recovery steps to the poly-SiGe resistor. The sequence consisted of first trimming the resistor with an approximate 4.0-s linear current sweep to 14.0 mA/μm^2. The resistor was then recovered by applying a recovery current of 11.7 mA/μm^2 (which corresponds to the experimentally measured maximum recovery current value for these resistors, [12]) for a total time of 40 000 s. The process was repeated several times and included trimming the resistor to different values by using current sweeps to 14.0 mA/μm^2 ($\sim$10% trim), 14.7 mA/μm^2 ($\sim$20% trim), and 15.7 mA/μm^2 ($\sim$30% trim). All recovery steps were done at 11.7 mA/μm^2 for a total time of 40 000 s. The results lead to two key conclusions. First, the trim process is reversible which indicates that dopant atoms segregate to the grain boundaries during resistor trimming (melting at grain boundary regions) while dopant atoms diffuse from the grain boundaries to the grains during recovery due to Joule heating [11], [12]. Second, although the polycrystalline Si/SiGe stack may be under mechanical stress due to the difference in the lattice constants of silicon and the SiGe alloy, there is no difference in the ability to trim these films electrically compared to conventional polysilicon films.

IV. Conclusion

Precision electrical trimming of stacked Si/SiGe polycrystalline resistors has been demonstrated for the first time. In addition to altering the resistance, the electrical trim process modifies the TCR such that it varies linearly with the percent of poly-SiGe thin film resistance trimmed. These results are consistent with those obtained on heavily doped polysilicon resistors, suggesting the trim/recovery process in poly-SiGe resistors are dominated by dopant segregation/diffusion mechanisms. Because the electrical trim/recovery process in stacked Si/SiGe polycrystalline resistors is similar to that in polysilicon resistors, it can be concluded that the introduction of a strained SiGe layer does not cause any disadvantage with regard to trimming these resistors.

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