Delay Time Studies and Electron Mobility Measurement in an a-Si:H TFT

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Abstract—**The time delay in the drain current response to a step in the effective drive voltage has been studied as one of the key parameters in characterizing the dynamic response of an a-Si:H thin-film transistor (TFT). It was determined that the a-Si:H delay time shows a similar behavior to that observed in a Si-MOSFET, i.e., it is directly proportional to the square of the channel length and inversely proportional to the effective drive voltage. A unique value of the channel field-effect electron mobility has been measured by employing the delay time results in the transmission line model. In amorphous semiconductors, the conventional methods of measuring mobility are inconvenient and complicated, whereas in this method the channel mobility is obtained by measuring only the delay time and the threshold voltage. Both of these parameters are obtained though electrical measurements on TFT's and hence require no special device structures.**

I. Introduction

HYDROGNEATED amorphous silicon (a-Si:H) is finding increasing application in several solid-state devices such as thin-film transistors (TFT's), solar cells, solid-state image sensors, charge-coupled devices, and many others [1]. The a-Si:H TFT has been used as an on-board switching element for "large-area electronics" such as flat-panel liquid-crystal displays and facsimile devices. Recently, the development of TFT logic circuits has become an important issue to commercial applications since the logic circuits adjacent to the TFT switching matrix will reduce the cost and improve the reliability of the flat-panel display. Therefore, characterizing, modeling, and improving the dynamic performance of the a-Si:H TFT has become critical to its many applications.

The principle of operation of a TFT is similar to that of a single-crystalline Si MOSFET, both of them being field-effect devices. However, the a-Si:H TFT and the MOSFET are distinctly different in their material properties. The high density of localized states in the bulk semiconductor and at the semiconductor–insulator interface degrades the performance of a TFT as compared to a MOSFET. Due to the similarity in their structures, the channel capacitance effects of a MOSFET are present in the TFT as well. The distributed channel capacitance of the MOSFET creates a time delay in the drain current response to a step change in the effective drive voltage. This distributed channel capacitance has been modeled as a transmission line by Burns [2]. In our study, the dynamic behavior of an a-Si:H TFT has been characterized by measuring the delay time dependence on the channel length and effective drive voltage. The delay time behavior in the TFT was found to be similar to that of a MOSFET. The similarities in the distributed channel capacitance and in the delay time behavior led us to extend the MOSFET transmission line model to the a-Si:H TFT.

The time of flight technique for measuring the active channel mobility requires special test structures and equipment. The more conventional conductance technique requires knowledge of the permitivity of the gate insulator, which is difficult to obtain for plasma deposited silicon nitride or silicon dioxide films. It also requires that the current be proportional to the square of the gate voltage in saturation, which may not be true. To obtain the mobility from the transmission line model, the only parameters to be determined are the delay time and the threshold voltage of the device. These parameters can be obtained through simple electrical measurements alone. Hence, this is a convenient method of measuring the channel field-effect electron mobility.

The purpose of this paper is to present the dependence of delay time on the channel length and the effective drive voltage for the a-Si:H TFT. Secondly, we show that a unique value of the channel field-effect electron mobility can be obtained from the model. This value of mobility was in general agreement with values obtained by conventional techniques, as reported in literature [3], [4].

II. Delay Time Studies

A. Experimental Details

Devices fabricated for normal circuit applications have channel lengths of about 5 μm. The delay time in these devices is of the order of fractions of a microsecond. Since parasitic elements such as lead inductance, transistor case capacitance and stray reactances associated with the physical configuration of the testing circuit dominate the measured response in these time scales, it becomes difficult to determine the actual device performance. To avoid this difficulty, test devices with long channel lengths, ranging from 25 to 200 μm, were designed and fabricated. The

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TFT has an Al–Si gate with the SiN_x and a-Si being deposited by plasma-enhanced chemical vapor deposition. Phosphorus ion implants were used for the source and drain contacts, but the channel itself was formed in intrinsic a-Si. Fig. 1 shows the cross section.

The circuit used to measure the delay time has the gate grounded and the source pulsed to a negative step voltage, which is the "drive voltage." The "effective drive voltage" is given by subtracting the threshold voltage from the drive voltage. The drain current response is measured by a digitizing oscilloscope connected across the drain resistor R_D. Care should be taken in adjusting the value of R_D because if it is too large then the parasitic response will dominate the device response. If R_D is too small, then the voltage drop will be too small to measure, since the currents are in the microampere range. This experimental setup is equivalent to pulsing the gate and the drain simultaneously to a positive voltage. When the source is pulsed negatively so that the gate is biased for electron accumulation in the channel of the TFT, the time taken for voltage pulse to travel from the source end to its drain end is measured as the delay time. Test devices were fabricated with five different channel lengths, i.e., 25, 50, 100, 150, and 200 μm with the width being 950 μm for every device. The delay time in each device was measured for five different gate voltages ranging from 10 to 19 V.

B. Results and Discussion

In a previous study we showed that unlike a MOSFET, the current–voltage relationship of an a-Si : H TFT, in saturation, is not necessarily a square law [5]. The drain current variation with the gate voltage is actually determined by the localized states and the a-Si-insulator interface though a parameter defined as η. This parameter was used to characterize the I–V dependence as $I_D \alpha (V_G - V_T)^{\eta}$ in saturation. If the density of tail states at the interface is expressed as

$$N_S = N_{SO} e^{\beta(E - Eo)} \tag{1}$$

then η is given by

$$\eta = (0.95\, q/kT\beta) + 1. \tag{2}$$

Different deposition conditions of the insulator and semiconductor result in different bulk and interface properties, hence different values of η. The results of the delay time studies for the case of devices exhibiting η of about 2 and the case when η was different than 2 are presented.

1. Threshold Voltage Measurements: The static transfer characteristics of one of the devices is shown in Fig. 2. In the voltage range from 0 to 5 V, the device characteristic varies exponentially. Over the gate voltage range from 10 to 20 V, the drain current goes as nearly the square of the gate voltage. Since the drain current variation, in most of the test devices followed nearly a square relationship with the gate voltage in saturation, the threshold voltage V_T was obtained by drawing a tangent to the $(I_D)^{1/2}$ versus $V_G (= V_D)$ curve. The tangent line

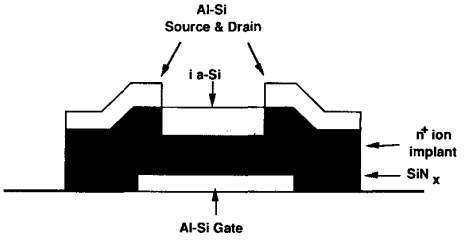


Fig. 1. Cross section of the a-Si : H TFT test device.

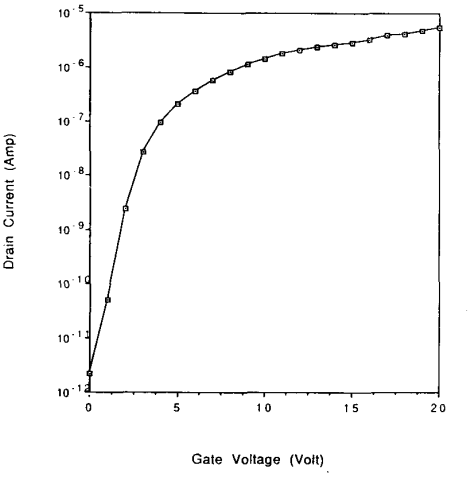
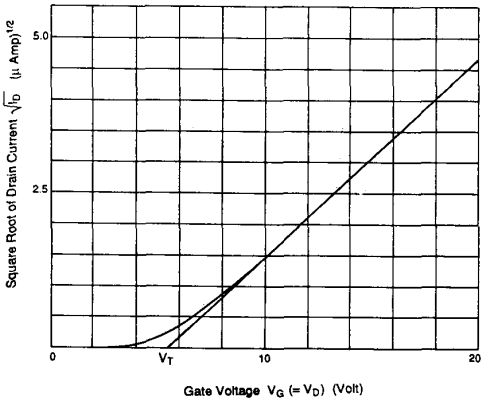


Fig. 2. I_D–V_G characteristics of a TFT with L = 50 μm and W =950 μm at a drain voltage of 2 V.

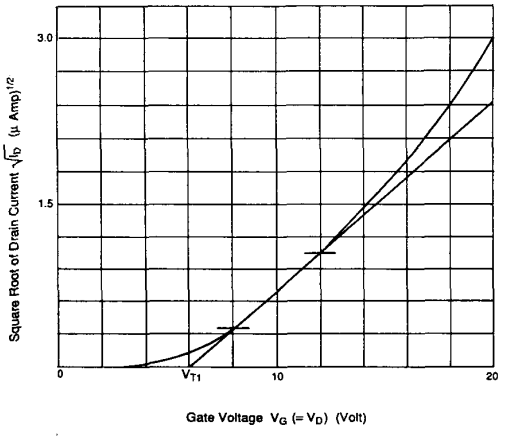
was extrapolated to the x axis to obtain V_T. Fig. 3(a) shows the $(I_D)^{1/2}$ versus $V_G (= V_D)$ plot for one such square-law device.

The drain current characteristics of a differently fabricated TFT with a channel length of 50 μm showed $\eta >$ 2. In this case, the drain current was treated as a piecewise square function with a different threshold voltage for each segment. The concept of variable threshold voltage can be explained as follows. As the voltage applied to gate of the TFT is increased, more charges are trapped at the interface and in the bulk amorphous silicon, shielding a greater part of the applied field from the channel. Hence, a larger gate voltage has to be applied to achieve the same accumulation. This effectively means an increase in the threshold voltage with increase in the gate voltage. V_T in each region of applied gate voltage was individually determined by drawing tangents to different segments of $(I_D)^{1/2}$ versus $V_G (= V_D)$ plot. Fig. 3(b) shows this plot for the 50-μm nonsquare-law device. V_{TI} is the threshold voltage obtained by drawing a tangent to the curve in the V_G range of 8 to 12 V.

2. Measurement of Delay Time: The delay time of TFT was measured using a digitizing oscilloscope. Fig. 4 shows the voltage drop across the drain resistor when the source voltage is pulsed. The initial voltage spike is due to the device parasitic capacitance and resistance (this initial transient can be reduced if self-aligned TFT structures



(a)



(b)

Fig. 3. $(I_D)^{1/2}$ versus V_G(= V_D) plot for (a) square-law device, (b) nonsquare-law device.

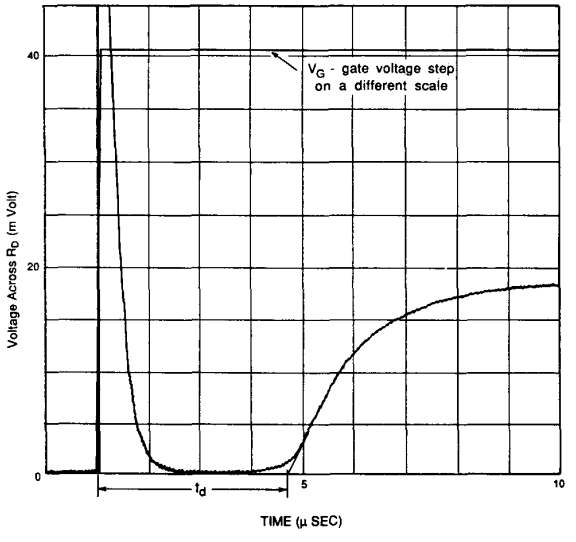


Fig. 4. Drain current response of an a-Si:H TFT with L = 25 μm measured across R_D at V_G-V_T = 5.6 V.

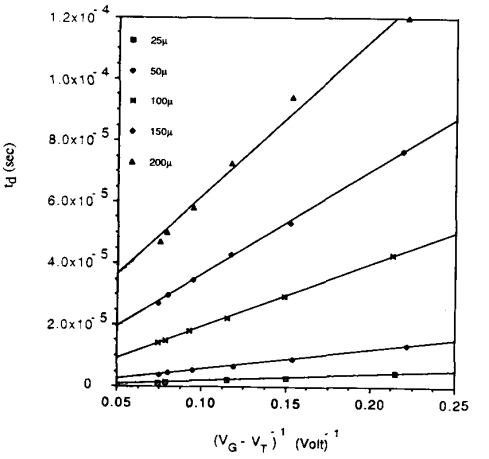


Fig. 5. The plot of the delay time t_d versus $1/(V_G - V_T)$ square-law devices with different channel lengths. The points are the experimental values. The lines are least square fit lines through these points.

are used). Once the initial transient has decayed , the actual device response voltage starts to rise and reached a steady state value. As can be seen from Fig. 4, there is a finite time delay between the instant when the source voltage is pulsed and when the response starts to appear at the drain terminal.

Fig. 5 shows the plot of measured delay time t_d versus $1/(V_G - V_T)$ for the square-law devices with different channel lengths. The valued of V_T for each particular channel length, measured earlier, was incorporated into the plot. Lines of least square fit were drawn through the data points. It can be seen that the experimental values are very close to the least square fit line. Hence, we conclude that the delay time is inversely proportional to $(V_G - V_T)$ in the case of square-law devices.

Fig. 6 shows the plot of t_d versus $1/(V_G - V_T)$ for the nonsquare-law device. The different values of V_t were incorporated in this plot by using the appropriate V_T according to the region of applied V_G. As can be seen the least square fit line agrees very well with the experimental data. Hence, the time delay is proportional to $1/(V_G - V_T)$, even in nonsquare law devices, if V_T is treated as a function of the applied gate voltage.

It is also desirable to examine the variation of the delay time with the channel length. The delay time was plotted versus the square of the channel length at four different $(V_G - V_T)$ values as shown in Fig. 7. The data points agree well with the least square fit lines and hence the time delay is proportional to the square of the channel length.

To summarize, the time delay in the a-Si:H TFT is found to be directly proportional to the square of the channel length and inversely proportional to the effective drive voltage

$$t_d \propto \frac{L^2}{V_G - V_T} \tag{3}$$

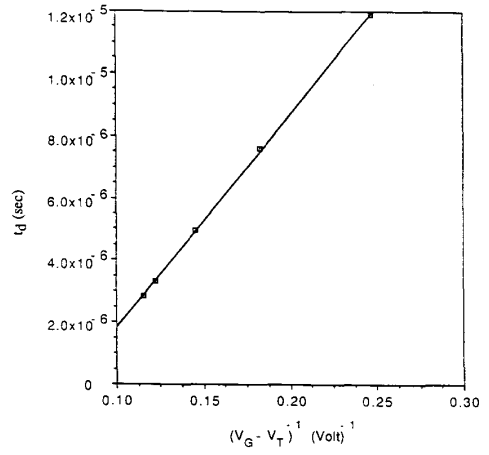


Fig. 6. The plot of the delay time t_d versus $1/(V_G - V_T)$ for the nonsquare law device. The points are the experimental values. The line is least square fit line through these points.

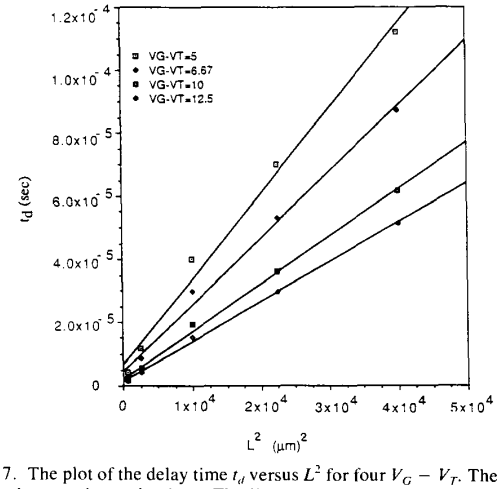


Fig. 7. The plot of the delay time t_d versus L^2 for four $V_G - V_T$. The points are the experimental values. The lines are least square fit lines through these points.

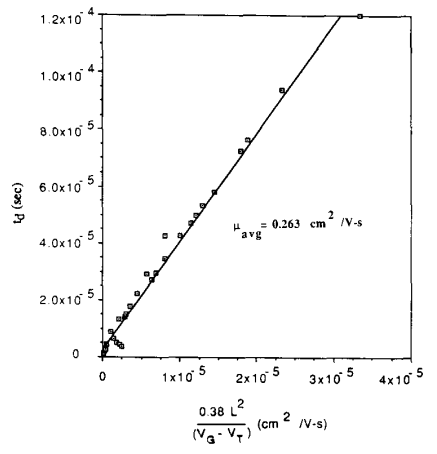


Fig. 8. The plot of the delay time t_d versus $0.38\ L^2/(V_G - V_T)$. The slope of the least square fit line gives the value of the average mobility.

The high-frequency performance of a MOSFET has been studied by Burns [2]. In his work the MOSFET active channel was modeled as a transmission line in which the insulator capacitance per unit length is a constant and the channel resistance per unit length is a function of the induced charge and thus of the voltage at that particular point. The voltage at any point along the channel is function of both the time and the distance from the electrode. Hence the time delay can be physically interpreted as the finite time it takes the current to charge up the distributed capacitance of the channel. Using the transmission line equations, the delay time between the instant when the source is pulsed and when the response appears at the drain was determined as (4):

$$t_d = \frac{0.38L^2}{\mu(V_G - V_T)}. \tag{4}$$

The above expression has been derived under the same bias conditions as used in this paper. In addition the mobility was assumed to be a constant, independent of the electric field in the channel. The active channel of the TFT has distributed channel capacitance and resistance effects similar to a MOSFET. In addition, as seen from our study, the time delay is proportional to $L^2/(V_G - V_T)$. Hence, the MOSFET transmission line model was applied to the TFT. However, the influence of the series source/drain resistances and contact resistances present in the TFT have not been included here. Using this model the channel field effect electron mobility can be obtained by measuring t_d and V_T.

All the experimental data points in Fig. 5 were combined to plot t_d versus $0.38\ L^2/(V_G - V_T)$. The surface electron mobility was determined from the slope of the least square fit line through these data points as shown in Fig. 8 to be 0.263 $cm^2/V\text{-}s$. This value of mobility is very reasonable and is in general agreement with the values obtained by other methods reported in literature. Although mobility, in general, is a function of the normal and tangential electric fields [6], an average value for a given voltage range can be conveniently obtained from this method.

IV. Conclusions

The purpose of this paper was to show the delay time dependence on channel length and effective drive voltage for an a-Si:H TFT. To obtain more accurate measurements of the delay time, very long channel TFT's were fabricated. The delay time was found to be proportional to the square of the channel length and inversely proportional to the effective gate voltage. The MOSFET transmission line model was extended to the TFT to obtain a value for the channel field effect electron mobility. This technique offers a very convenient way of measuring the electron mobility since the only two parameters needed are the the delay time and threshold voltage. Both these parameters can be determined easily through electrical

measurements alone and do not require special instrumentation. The technique of measuring mobility can be used for TFT's exhibiting any functional I–V dependence.

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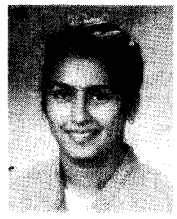

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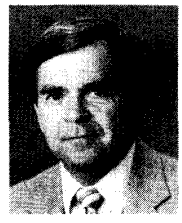

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