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High sensitivity acoustic transducers with thin p + membranes and gold back-plate

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Abstract

High sensitivity acoustic transducers (microphones) have been fabricated on 5″ wafers in a production environment and the experimental results are presented. One of the main advantage of this microphone design is that it can be fabricated on a single wafer eliminating the need for the multiple wafers and subsequent wafers bonding steps as in conventional designs. The devices use thin (~3 μm) p + silicon membranes as the active movable element and a thick perforated plated gold back plate. The p + membranes are fabricated using an optimized boron solid source diffusion at 1150°C. Ethylene–Diamine–Pyro-Catecol (EDP) etching at 100°C was performed from the backside of double-sided polished wafers to release the thin silicon membranes. The zero-bias capacitance with the air gap was 2.2 pF and it increased to 2.4 pF at 9 V. The frequency response was measured and the measured sensitivity of 5.28 mV/Pa at 5 V and 10.77 mV/Pa at 9 V at 1 kHz are among the highest reported in literature for micro-machined acoustic transducers.

Keywords: Acoustic transducers; Silicon microphones; Micro-machining

1. Introduction

Silicon micro-electro-mechanical-system (MEMS) technology has been used to produce a variety of systems-on-a-chip in the consumer, automotive, biomedical, and industrial market segments [1]. Numerous pressure sensors have been reported in literature. Acoustic transducers, which can be considered a special class of pressure sensors, have been made in silicon. The key features of introducing silicon technology for these applications include; (i) a very high degree of control of dimensions, (ii) miniaturization of the devices and mechanical elements, (iii) the possibility of batch fabrication and hence the subsequent reduction of cost from economies of scale, and (iv) integration of the acoustic transducers with integrated circuits, e.g., CMOS to make a system-on-a-chip. All of these factors help in improving the cost–performance product for these acoustic devices.

The condenser type capacitive microphones sense the capacitance change due to the external excitation, i.e., sound pressure. The gap between a fixed plate and a movable plate in the device changes with the sound waves and thereby changes the capacitance. This change in capacitance will be directly proportional to the applied external force. Since the first attempt by Royer et al. [2] to fabricate acoustic transducers, many reports have been made using two bonded wafers for acoustic transducers [3,4]. In 1991 Scheeper et al. avoided the use of an extra wafer for the back plate by using a sacrificial layer and gold plating to fabricate the back plate on the same wafer with the diaphragm [5]. Bernstein et al. have reported earlier versions of the devices produced in this paper [6]. Pedersen et al. have reported condenser microphones fabricated by micro-machining of polyimide on silicon substrates with integrated voltage converters and preamplifier detection circuits [7,8]. The purpose of this paper is to report the fabrication and results of very high sensitivity acoustic transducers fabricated using surface and bulk silicon micro-machining techniques in a manufacturing environment.

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The devices have been fabricated on 5″ wafers and exhibit much higher sensitivities at low voltage bias conditions (< 10 V) than previously reported [6].

2. Device fabrication

The silicon microphone described here is a condenser type capacitive microphone. The basic movable element is a thin (~ 3 μm thick) diaphragm made from p+ silicon. The p+ silicon is one side of an air gap capacitor. The p+ regions are formed using boron solid source diffusion at high temperatures. The other plate of the capacitor is a 20 μm thick perforated gold back plate formed using electroplating. The air gap is defined using a 2.2 μm thick sacrificial photoresist. The wafer is etched from the backside using a wet etch to stop on the p+ diaphragm. Air pressure moves the thin p+ layer and causes a capacitance change due to change in the distance between the thin p+ layer and the thick Au back plate. The change in capacitance is detected by a JFET buffer chip adjacent to the microphone in the same package.

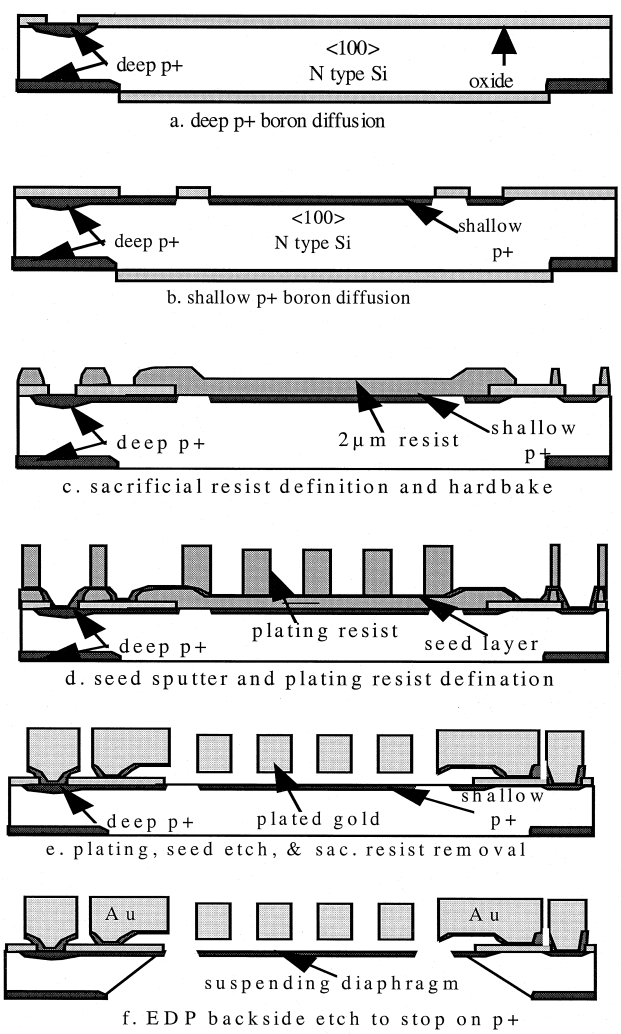

Fig. 1. Cross-section process flow of the silicon micro-machined microphone.

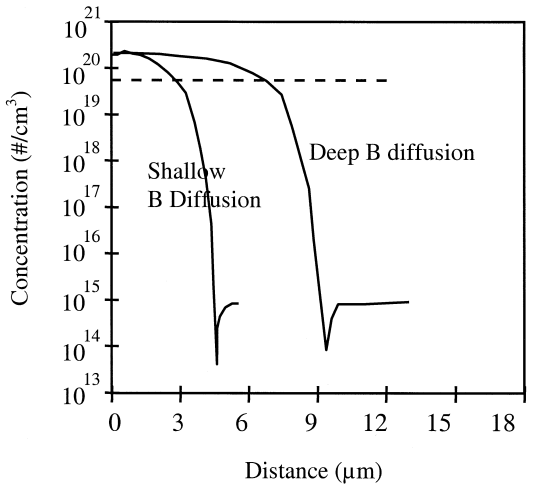

Fig. 2. Final spreading resistance profile of the deep and shallow boron diffusion.

The process begins on N-type double side polished wafer with thermally grown initial oxide of 8000 Å. Deep boron diffusion areas (for diaphragm springs) were defined by using photoresist mask and dry/wet etching of oxide on the front side of the wafer. Windows were also defined on the backside of the wafer and solid source boron diffusion was done at 1150°C for 3 h at 1% O_2 as shown in Fig. 1(a). Next, a masking oxide was grown on the p+ areas and a 90 min anneal at 1150°C in 10% O_2 was done to further activate the boron and reduce stress in the p+ layer. Then, shallow boron diffusion areas for the thin membranes were defined using photoresist mask and wet etching of oxide. A 6000 Å undoped oxide from a TEOS (Tetraethylorthosilicate) source was deposited at the back of the wafer to protect the back from subsequent boron diffusion. The shallow boron diffusion was done at 1125°C for 50 min in 1% O_2. A thin oxide (~ 1000 Å) was grown on the wafer and striped from the back of the wafer. A rapid thermal anneal (RTA) cycle was performed at 1100°C for 20 s to eliminate stress and damage in the p+ doped areas. The cross-section at this step is shown in Fig. 1(b).

Contact windows were etched through the field oxide and the thin oxide on the boron doped areas were opened by wet etching in a buffered hydrofluoric acid solution. Using a photoresist mask, substrate contact areas were implanted by Arsenic with dose of 1×10^{15}#/cm^3. After a short implant annealing step, an undoped oxide (~ 1000 Å) from a TEOS source was deposited at the back of the wafer. Subsequently, a 2.2 μm thick photoresist was patterned on the front of the wafer. The thickness of this resist will define the spacing between the back plate and the silicon diaphragm. In other words, this photoresist layer will act as a sacrificial layer during the surface micro-machining to form the back plate suspended on the top of the

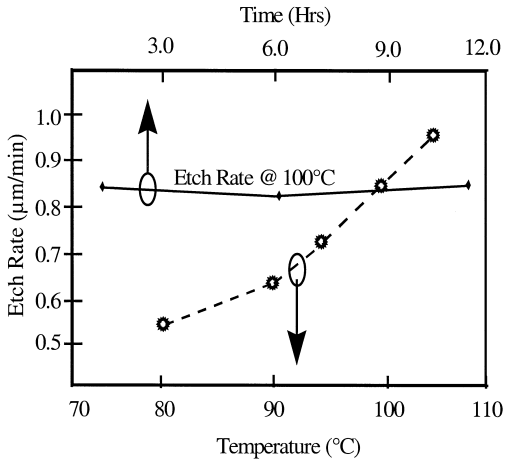

Fig. 3. Etch rate of the EDP etch. Solid line shows etch rate as a function of time at 100°C. Dashed line shows the etch rate as a function of temperature.

moving diaphragm. The cross-section at this step is shown in Fig. 1(c).

The process then commenced with the plating module. Seed layers (Ti/Ni) were sputtered and a thick photoresist (AZ4620) was patterned to form the mold for the subsequent gold plating at the front of the wafer as shown in Fig. 1(d). A 20 μm thick Au was plated in gold sulfite bath at 50°C for 120 min. After plating, another layer of thick photoresist was spun on the front of the wafer and the oxide from the back was etched away completely by a buffered hydrofluoric acid solution. Next the plating resist was striped and the seed layers were etched to expose the underlined spacer photoresist. This sacrificial spacer photoresist was then removed in a solvent. The wafers were finally etched in EDP (Ethylene–Diamine–Pyro-Catecol) solution at 100°C for 9 h to release the membranes. Fig. 1(f) shows the final cross-sectional diagram.

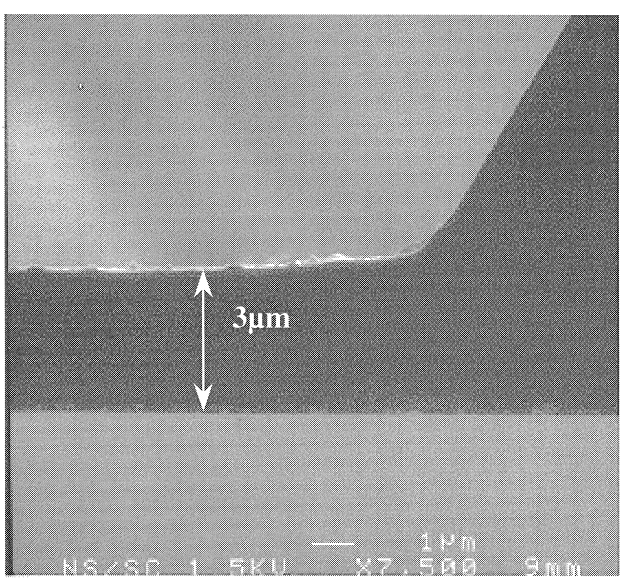

Fig. 4. SEM cross-section of the final thin p+ silicon membrane.

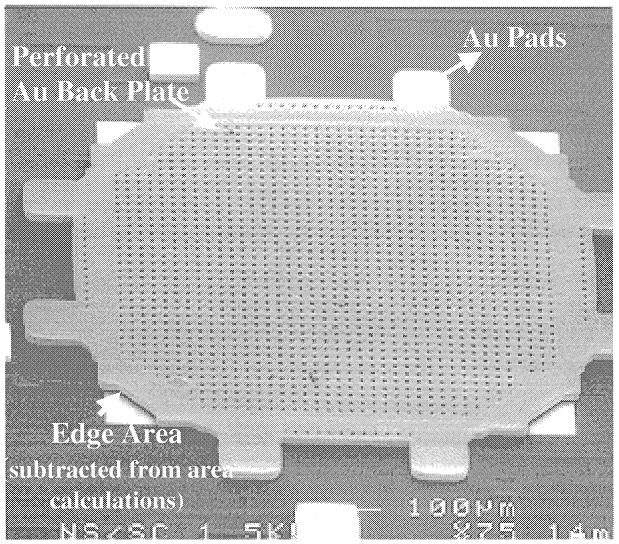

Fig. 5. Top view SEM photograph of the micro-machined silicon condenser microphone.

The spreading resistance profiles in Fig. 2 show the junction depth and boron concentration after the deep and the shallow boron diffusion. The junction depth at 8×10^{19}#/cm^3 was about 3 μm for the shallow diffusion and about 7 μm for the deep diffusion. EDP was chosen as the wet etchant due to its high selectivity to p + doped silicon. The etch rate was characterized in EDP from 70°C to 110°C. The high selectivity is critical since the etchant is also attacking the silicon from the topside of the membrane. In addition, Au is also exposed during the etch and EDP has a very high selectivity to Au. The etch rate varied between 0.55 μm/min to about 1.0 μm/min when the temperature was changed from 70°C to 110°C. The etch was performed in a re-circulating bath with precise temperature control. Fig. 3 shows the measured etch rate characteristic of the EDP on 100-oriented N-type silicon as a function of temperature. The variation of etch rate of silicon during a 12 h long etch was negligible as shown in

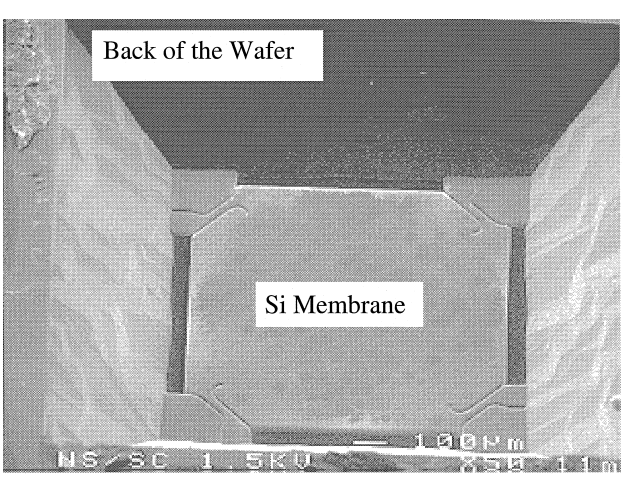

Fig. 6. SEM photograph showing silicon membrane from the back of the wafer after the EDP etch.

Fig. 3. These results were consistent with literature. The silicon was finally etched using EDP at 100°C for 9 h.

3. Results

Fig. 4 shows the SEM of the final thin membrane after the EDP etch showing a thickness of about 3 μm. Fig. 5 shows an SEM angled top view of the Au back plate of the fabricated silicon micro-machined microphone. Fig. 6 shows the backside etch cavity formed by the EDP etch. After the completion of the backside etch, electrical testing was performed. The initial electrical test that would indicate if the device is 'not' functional is the measurement of the DC current vs. the DC voltage applied between the silicon membrane and the gold back plate. The presence of a large leakage current would indicate a short between the two plates of the capacitor. Similarly, an absence of the snap down voltage would indicate the presence of an unwanted material (e.g., resist or other contaminants) between the two plates. Repeated voltage sweeps show a snap down voltage of ~14 V as shown in Fig. 7 indicating DC functionality. Next, the capacitance vs. voltage characteristics were measured and are shown in Fig. 8. The zero bias capacitance, corresponding to an air gap of about 2.2 μm (defined by the resist) was 2.2 pF. Thus the effective overlap area of the parallel plate capacitor was about 5.45×10^5 μm^2. The expected capacitance should be from the overlap area of the p+ silicon diaphragm and the Au back plate in addition to any parasitic capacitance between the Au back plate and the substrate in the field oxide region. The overlap area is given by;

$$A_{\text{overlap}} = A_{\text{Si\_diaphragm}} - A_{\text{hole}} \times \text{number of holes} - A_{\text{edge}}$$

(see Fig. 5)

Thus $A_{\text{overlap}} = 850 \times 850\ \mu\text{m}^2 - 100 \times 1176\ \mu\text{m}^2 - 120 \times 120 \times 2 = 5.76 \times 10^5\ \mu\text{m}^2$. This number is within about 6% of the number calculated using the capacitance measurement and the difference could be due to layout and masking definition issues. The capacitance increased with increasing bias voltage due to the decrease in the air gap thickness as the p+ silicon membrane is electrostatically

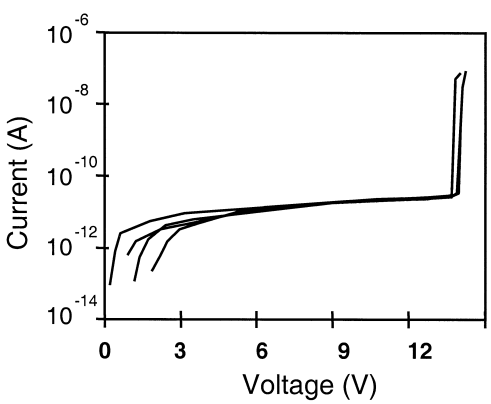

Fig. 7. $I-V$ plot showing repeated snap down curves.

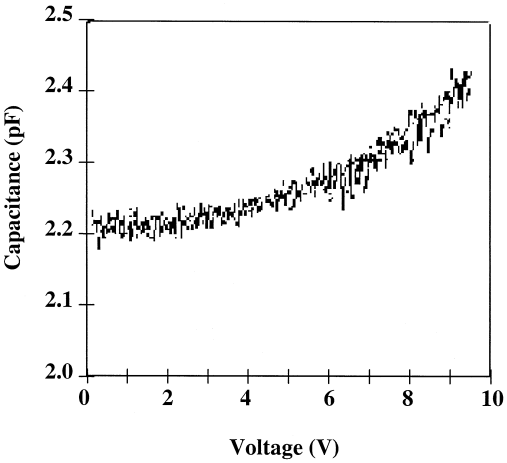

Fig. 8. Capacitance–voltage measurement results of a microphone. The maximum bias voltage is 70% of the V_{SD} (Snap Down Voltage).

pulled towards the Au back plate. The capacitance increased to 2.4 pF (a 10% increase) at 9 V. V-grooves formed during the anisotropic etch allow the microphones to be easily snapped apart and packaged for acoustic testing. A JFET buffer circuit with a 15 GΩ undoped polysilicon resistor was used inside the package to transfer the electrical signal from the microphone to the outside amplifier circuits.

The frequency response of the device was measured using an HP Dynamic Signal Analyzer. The sensitivity vs. frequency was measured in reference to a calibrated microphone with known characteristics and a sensitivity of 3.4 mV/Pa at 1 kHz. The measured sensitivity vs. frequency is shown in Fig. 9. The sensitivity was converted to decibels according to the formula;

$$\text{Sensitivity}\,(\text{dB}) = 20 \times \log_{10}\left[\frac{\text{Sensitivity}}{3.4\,\text{mV/Pa}}\right]$$

Typical devices show a very flat response and sensitivities of up to 10.77 mV/Pa at 1 kHz and 9 V, which is

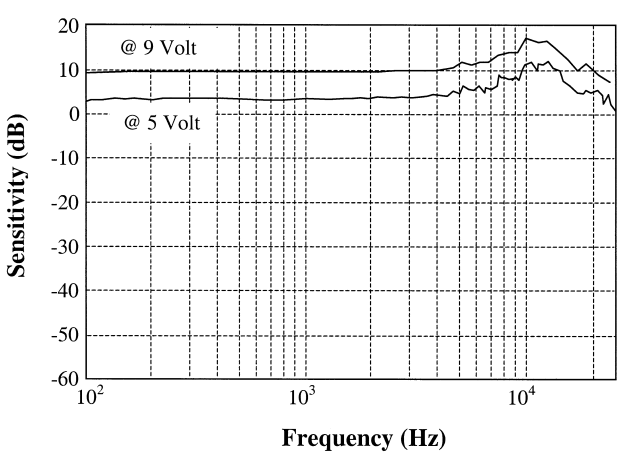

Fig. 9. Plot of sensitivity of the microphone vs. frequency for the silicon microphone at 5 V and 9 V across the air gap. The sensitivity was normalized and referenced against a commercial microphone with sensitivity of 3.4 mV/Pa at 1 kHz.

about 65% of the maximum allowed voltage. Even at 5 V (about 35% of the maximum allowed voltage), the sensitivity was 5.28 mV/Pa, which is one of the highest reported for such devices at such a low voltage operation.

4. Conclusions

A silicon micro-machined microphone has been fabricated with high sensitivity in a manufacturing environment. The devices used a thin p+ membrane as the movable element as one side of an air gap capacitor. A thick perforated Au plated back plate was used as the other side of the capacitor. The devices have a snap-down voltage of ~14 V. Very high sensitivities of up to 10.77 mV/Pa at 9 V and 5.28 mV/Pa for 5 V operations have been successfully demonstrated.

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References

[1] For a good overview of silicon micro-machining and related applications, see the special issue of Proceedings of the IEEE, Vol. 86, No. 8, 1998.
[2] M. Royer, J.O. Holmen, M.A. Wurm, O.S. Aadland, M. Glenn, ZnO on Si integrated acoustic sensor, Sensors and Actuators 4 (1983) 357–362.
[3] W. Kuhnel, G. Hess, Micro-machined subminiature condenser microphones in silicon, Sensors and Actuators A 32 (1992) 560–564.
[4] D. Hohm, G. Hess, A subminiature condenser microphone with silicon nitride membrane and silicon back plate, J. Acoust. Soc. Am. 85 (1989) 476–480.
[5] P.R. Scheeper, W. Olthuis, P. Bergveld, Fabrication of a subminiature silicon condenser microphone using the sacrificial layer technique, Proc. 6th Int. Conf. Solid-State Sensors and Actuators (Transducers '91), San Francisco, USA, June 24–28, 1991, 408–411.
[6] J.J. Bernstein, J.T. Borenstein, A Micromachined Silicon Condenser Microphone With On-Chip Amplifier, Technical Digest of the Solid State Sensors and Actuators Workshop, Hilton Head Island, 1996, pp. 239–243.
[7] M. Pedersen, W. Olthuis, P. Bergveld, Integrated silicon capacitive microphone with frequency-modulated digital output, Sensors and Actuators, A: Physical 33 (1998) 267–275.
[8] M. Pedersen, W. Olthuis, P. Bergveld, High-performance condenser microphone with fully integrated CMOS amplifier and dc–dc voltage converter, Journal of Microelectromechanical Systems 7 (4) (1998) 387–394.

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