Back-Gated Buried Oxide MOSFET's in a High-Voltage Bipolar Technology for Bonded Oxide/SOI Interface Characterization

R. Bashir, F. Wang, W. Greig, J. M. McGregor, W. Yindeepol, and J. De Santis

***Abstract*— A novel back-gated P-MOSFET structure is fabricated in a high-voltage complementary bipolar technology using BESOI (bonded etch back SOI) substrates. The P+ buried layer regions, used for the PNP BJT are used as the source and drain regions, the N- epi as the channel region, the silicon handle wafer as the gate, and the BOX (buried oxide) as the gate oxide. The P-MOSFET was used to characterize the interface between the BOX and the SOI. The devices exhibit high sub-threshold slope which is attributed to a high interface state density of about $2\times10^{12}\#/\text{cm}^2$ at the bonding interface. Bias-temperature stress measurements show an effective mobile charge density of $4\times10^{10}\#/\text{cm}^2$ in the buried oxide.**

I. Introduction

BONDED ETCH BACK SOI (BESOI) wafers are finding increasing use as start substrates for analog, deep submicron CMOS applications, and new MEMS technologies [1]–[3]. There has been rapid progress in BESOI manufacturing technology and a variety of substrates are now commercially available. The use of BESOI substrates to provide device isolation for a 170 V dielectrically isolated complementary bipolar technology has been recently reported [4]. While deep trenches provide lateral isolation, the use of SOI provides vertical device isolation for high voltages, eliminating the need for deep wells used in previous technologies [5]. The integrity of the BOX and BOX/SOI interface is critical in providing a robust and reliable high voltage isolation.

The purpose of this work is to describe a P-MOSFET structure which is fabricated in a dielectrically isolated complementary bipolar technology without additional masking steps. The device is very useful in characterizing the quality of the buried oxide and the BOX/SOI interface and can also be fabricated in thin SIMOX or other SOI substrates.

II. Process Flow and Electrical Results

BESOI substrates with 2.5 μm 1–4 Ω-cm N-type SOI and 1 μm (or 0.5 μm) BOX were used. The detailed bipolar process flow is described elsewhere [4]. In summary, N+/P+ buried layers were implanted, and driven for the BJT's. A 16 Ω-cm, N-type epitaxial layer was grown to a thickness necessary for the achieving the required breakdown voltages. Heavily doped regions (sinkers) were formed from the top down to form low resistance contacts to the BJT's. Deep trenches were used to provide lateral isolation.

Fig. 1 shows a drawn cross section of the P-MOSFET. The P+ buried layers were used to make the source/drain regions. The P+ sinker regions were used to provide top contacts to the P+ source/drain regions. The source/drain regions intersect the deep trench sidewall. However, since the source to drain leakage is low, there is no parasitic channel along the trench sidewall. Since the gate bias is being applied to the substrate and the silicon outside the device is grounded, negligible variation in the parasitic trench sidewall channels is assumed. The channel was formed at the bonded oxide/SOI interface. $I_{\rm D}$ versus $V_{\rm G}$ characteristics were measured at $V_{\rm DS}=10$ V and $V_{\rm B}=0$ to extract the sub-threshold slope as shown in Fig. 2. The subthreshold slope is given by [6]

$$\text{S}\sim 2.3\frac{kT}{q}\left(1+\frac{C_{\rm d}+C_{\rm it}}{C_{\rm ox}}\right) \tag{1}$$

where $C_{\rm d}$ is the depletion capacitance in the silicon, $C_{\rm ox}$ is the gate oxide capacitance, and $C_{\rm it}(=qD_{\rm it})$ is the interface state capacitance. $C_{\rm d}$ can be calculated knowing the doping profile in the SOI. For high values of S, $C_{\rm it}$ dominates (1) above. Using S = 2.94 and $T_{\rm ox}=0.5$ μm, $D_{\rm it}$ can be calculated to be 2.04e12#/eV-cm^2. Using S = 6.5 and $T_{\rm ox}=1.0$ μm, $D_{\rm it}$ can be calculated to be 2.29el2#/eV-cm^2. The two values are close and within measurement and formulation accuracy. The high value of $D_{\rm it}$ is expected since the channel is formed at the interface of bonding during the BESOI substrate manufacturing.

Fig. 3 shows the $\text{S}_{\text{qrt(ID)}}$ versus $V_{\rm G}$ curves for $T_{\rm ox}=0.5$ μm and 1.0 μm. From the slopes of the line, $\mu_{\rm h}=138$ cm^2/V-s for device with $T_{\rm ox}=0.5$ μm and $\mu_{\rm h}=13$ cm^2/V-s for device with $T_{\rm ox}=1$ μm. The value of $\mu_{\rm h}$ is reduced in the later case due to gate induced electric field degradation since this value is extracted at $V_{\rm G}$ which is about four to five times the value of $V_{\rm G}$ used to extract the slope and $\mu_{\rm h}$ for the device with $T_{\rm ox}=0.5$ μm.

Bias-temperature stress measurements were also performed at $V_{\rm G}=0$ and 200 °C and then at $V_{\rm G}=50$ V for 5 min at 200 °C and $V_{\rm G}=50$ V for 5 min at 200 °C. Transfer

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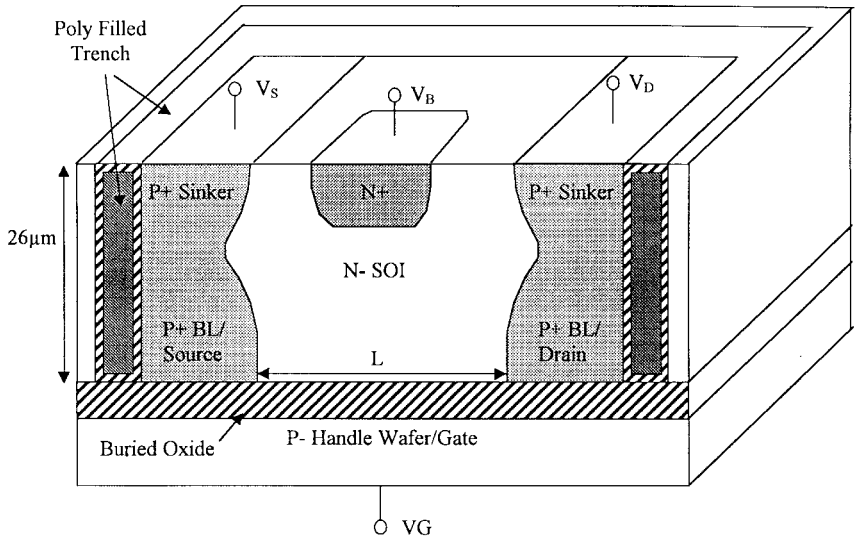

Fig. 1. Cross section of the P-MOSFET. Channel length L = 31 μm; channel width W = 158 μm.

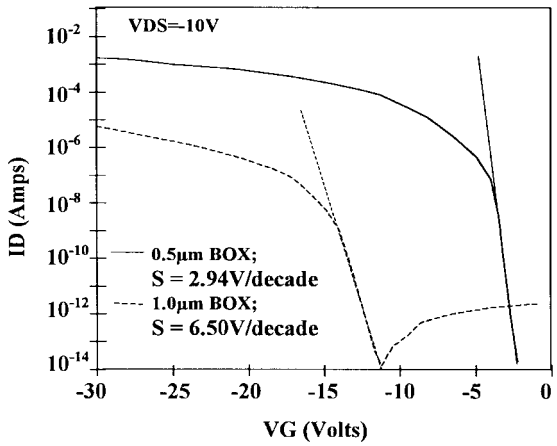

Fig. 2. I_D–V_G transfer characteristics of the SOI P-MOSFET with 0.5 μm and 1.0 μm BOX used to extract the subthreshold slope.

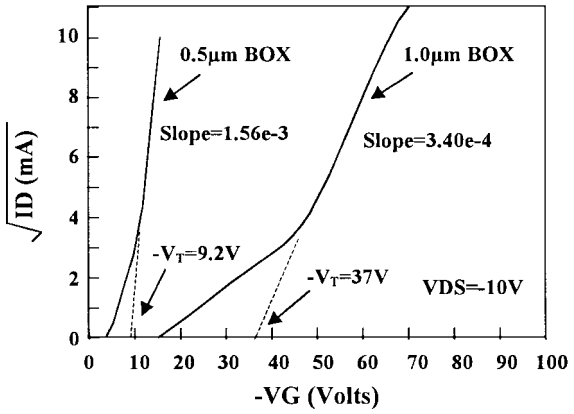

Fig. 3. $S_{qrt}(I_D)$ versus V_G characteristics showing V_T and slopes of lines used to calculate μ_h.

characteristics were measured at each of the above bias-temperature stress point. As shown in Fig. 4, a shift of about 1.9 V can be seen after the positive bias stress indicating an effective mobile oxide charge density of $4.1\times10^{10}\#/\text{cm}^2$. The

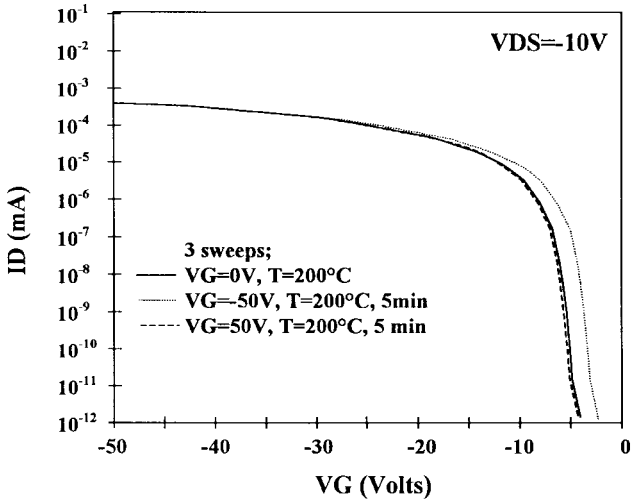

Fig. 4. Bias-temperature stress characteristics of the bonded oxide P-MOSFET showing a shift in transfer curves of 1.9 V.

value of mobile oxide charge density is very low, indicating a good quality process and no inherent degradation or charge due to the buried oxide quality itself.

III. Conclusions

A novel BOX gate oxide SOI P-MOSFET fabricated in a high voltage bipolar technology is presented. The device can be used to characterize the BOX/SOI interface characteristics and the BOX quality. Sub-threshold slopes indicate a high density of states of $\sim$ 2e12#/eV-cm^2 at the SOI/bonded oxide interface. BTS measurements indicate mobile charge density of $4\times10^{10}\#/\text{cm}^2$ in the buried oxide. The device is very useful in characterizing the buried oxide quality and the SOI/buried oxide interface.

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