Elimination of the Sidewall Defects in Selective Epitaxial Growth (SEG) of Silicon for a Dielectric Isolation Technology

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***Abstract*—Selective epitaxial growth (SEG) of silicon has not had widespread use as a dielectric isolation technology due to the near sidewall defects at the SiO_2 silicon interface. These defects are located in the first 1–2 μm of the SEG/sidewall SiO_2 interface. Diode junctions intersecting the sidewall and 5 μm removed from the sidewall were fabricated in SEG material using thermally grown silicon dioxide (OX) and thermally nitrided thermal silicon dioxide (NOX) as the field insulating mask. Averaged over 16 devices of each type, diodes fabricated with NOX had much better low current I-V characteristics and minimum ideality factors (1.03) than diodes fabricated with OX field oxides (1.23). Junctions intersecting the NOX field insulator had nearly identical characteristics to bulk SEG.**

I. Introduction

PRESENTLY the main emphasis is producing smaller devices with less parasitic capacitance, that switch faster, and have increased packing densities. Trench and local oxidation of silicon (LOCOS), for the next generation of ULSI, have a number of drawbacks as device dimensions are further reduced. LOCOS has lateral oxidation or the bird's beak which reduces the active area and results in a nonplanar surface. In the case of CMOS, latch-up and cross-talk prevention requires larger spacing between MOSFET's. In the 1980's, the use of selective epitaxial growth (SEG) was proposed as a dielectric isolation technology that had a higher packing density [1], [2], eliminated the bird's beak, had no pad oxide or deposited nitride, and required no additional oxidation steps. As illustrated in Fig. 1, fabricating CMOS with SEG, up to the point where the N- and P-channel devices are produced, is a much simpler process than LOCOS. The wafer is first thermally oxidized (SiO_2), then patterned for the device areas, the oxide is etched, and then SEG is grown to slightly above the oxide. Chemical mechanical polishing (CMP) of the SEG, back to the local area field SiO_2 etch stop, provides a planar surface and removes all facets. The greatest barrier to wide spread use of SEG as an isolation technology and in the fabrication of small devices was the sidewall electronic quality. Devices fabricated in SEG material were measured to be as good as substrate devices only when all junctions were 1–2 μm from the sidewall [3]–[5]. When the junction intersected the sidewall, the low current I-V characteristics became degraded, with large leakage currents [4], [6], [7], lower breakdown voltages [1], and larger junction ideality factors. These defects have recently been determined to be due to stresses induced in the SEG during cool-down from the growth temperature. The large mismatch in the thermal expansion coefficients of silicon and the field SiO_2 was shown to be the cause [9], [10]. This paper reports for the first time a fabrication process for the near elimination of these sidewall defects in SEG and hence makes new device structures and a compact isolation technology possible.

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II. Diode Fabrication

Thermally nitrided thermal silicon dioxide (NOX) was used as the field insulator to reduce the differences ($SiO_2 < Si < Si_3N_4$) in the relative expansion coefficients between silicon and SiO_2($C_{T\text{-}Si} = 5.8 \times 10^{-6}/C, C_{T\text{-}SiO_2} = 5.0 \times 10^{-7}/°C$). Since Si_3N_4 has a larger C_T than silicon, a nitrided SiO_2 should have a closer match. The field oxide was formed on (100) silicon wafers using a dry O_2 at 1100°C for 2 h and then 10 min in steam to obtain 0.9 μm SiO_2 (OX). The NOX film was obtained by thermally nitriding the above SiO_2 in pure ammonia (NH_3) at 1100°C for 60 min. At this temperature, nitrogen is incorporated into the oxide and the thermal expansion coefficient is modified. After nitridation, SIMS profiles indicated it contained ~2–4 atm% of nitrogen [11], [12]. For defect comparison, both OX and NOX were used as the field dielectric. Fig. 2 illustrates the two types of diodes fabricated to measure the differences in sidewall defects. Note that one has a junction that intersects the sidewall (SEG) and the other is 5 μm from the wall (SEG-5). Seed windows for SEG were RIE or wet etched into both OX and the NOX wafers. RIE consisted of a 200 W, 80 mTorr, CHF_3 plasma etch followed by a 5 min, 1000°C steam oxidation to remove any damage. The wafers were dipped in BHF for 30 s to remove the native oxide and then n-type SEG was grown at 970°C, 40 Torr, with gas flows of SiH_2Cl_2 = 0.22 slpm, HCl = 0.56 slpm, H_2 = 60 slpm in a commercial CVD reactor with a growth rate of about

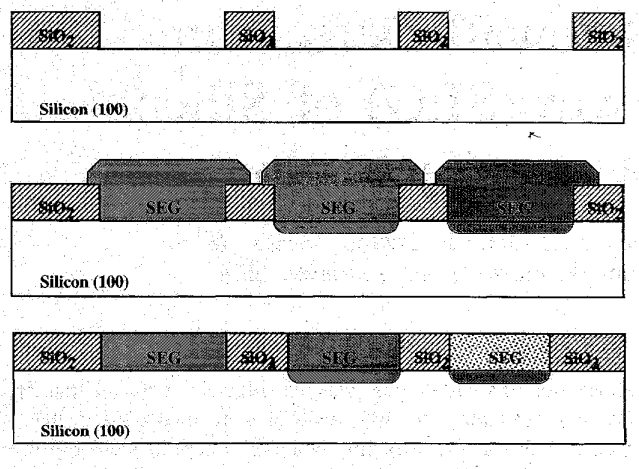

Fig. 1. Cross section of SEG as a dielectric isolation technology.

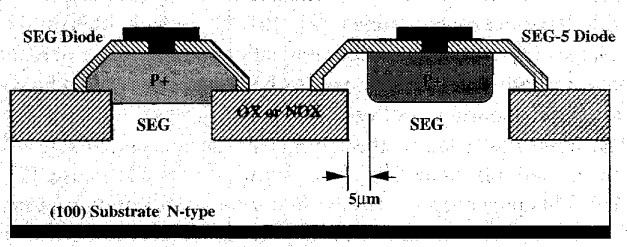

Fig. 2. Cross section of diodes where the junction intersects the sidewall (SEG) and diodes that have the junction 5 μm from the wall (SEG-5).

0.12 μm/min. Boron was implanted at an energy of 25 keV with a dose of 1×10^{14} cm^2 to create the p^+ regions, followed by a 10 min 1000°C anneal and then a Al-1%Si metallization step. A hydrogen anneal was then performed for 20 min at 475°C.

III. Experimental Results

Diode I-V and ideality factors were measured for each type of diode and each dielectric with a HP 4145B parameter analyzer. A total of 144 diodes, that had a range of areas and perimeters (16 devices), were measured. Diodes fabricated in the substrate, as process control devices, had an average minimum ideality factor (n) of 1.02 as listed in Table I. Those SEG diodes with wet etched thermal oxide (OX) as the insulator mask had excellent low current characteristics when the junction was 5 μm from the sidewall (OXSEG-5) with the average minimum ideality factor of near 1.00. When the junction intersected the SiO_2 sidewall (OXSEG), the average minimum ideality factor increased to 1.23 and the recombination currents increased significantly.

Diodes fabricated with NOX as the dielectric also showed excellent characteristics when the junction was at least 5 μm from the sidewall (NOXSEG-5) with the average minimum ideality factor of 1.03. Now, however, when the junction intersected the NOX sidewall (NOXSEG), the device I-V characteristics remained nearly the same and the average minimum ideality factor was essentially the same at 1.03. The I-V characteristics are shown in Fig. 3 for a typical NOXSEG and a NOXSEG-5 device with the same area and perimeter,

TABLE I
Average* Minimum Ideality Factor of SEG Diodes with Wet and Dry Etched Seed Windows

Insulator Type	Diode Type	Seed Wet Etch	Seed Dry Etch
N/A	Substrate	1.02	N/A
Thermal Oxide	OXSEG-5	1.00	1.02
Thermal Oxide	OXSEG	1.23	1.10
Nitrided Oxide	NOXSEG-5	1.03	1.15
Nitrided Oxide	NOXSEG	1.03	1.08

* 16 diodes of each type of each kind

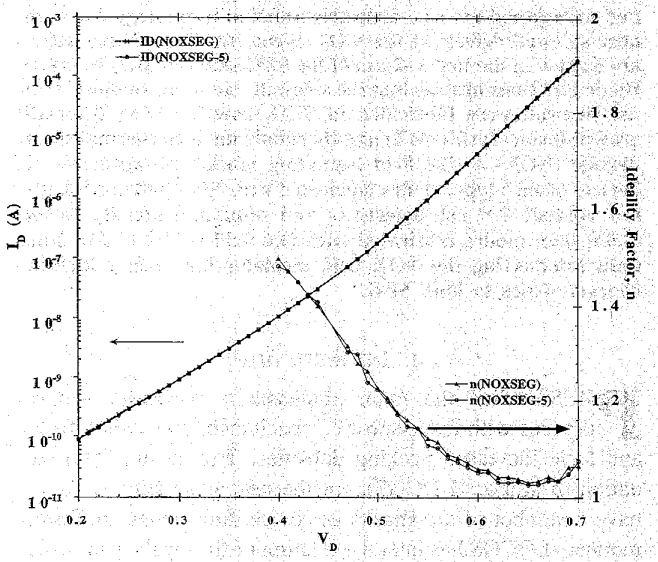

Fig. 3. I-V characteristics and ideality factor characteristics for NOXSEG and NOXSEG-5 diodes with wet etched seed windows.

indicating how closely they are matched, particularly in the low current region. Similar results were obtained for dry etched seed windows as shown in Table I where the diodes intersecting the sidewall were even a little better than the nonintersecting diodes.

IV. Conclusions

Diodes whose junctions intersected the SEG/thermally nitrided oxide sidewall showed nearly identical electrical characteristics to those 5 μm away from the wall and were very comparable to substrate devices and to the OXSEG-5 devices. Sidewall defects produced in SEG of silicon were essentially reduced to bulk levels, within experimental error, using a thermally nitrided thermal oxide as the field insulator, which in turn becomes the dielectric for a trench-like isolation technology. The drastic reduction in the sidewall defects is a result of the reduced stress placed on the SEG upon cool-down from the growth temperature.

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