

Degradation of Insulators in Silicon Selective Epitaxial Growth (SEG) Ambient

R. Bashir, *Member, IEEE*, S. Kim, N. Qadri, D. Jin, *Member, IEEE*, G. W. Neudeck, *Fellow, IEEE*, J. P. Denton, *Member, IEEE*, G. Yeric, *Member, IEEE*, K. Wu, and A. Tasch, *Fellow, IEEE*

Abstract—The degradation of various insulators in Silicon Selective Epitaxial Growth (SEG) ambient was studied. The insulators studied were thermal oxide, reoxidized nitride/oxide stack, poly-oxide, and nitrided oxide. Breakdown electric fields of MIS capacitors were measured and yields were calculated before and after the insulators were exposed to Silicon SEG ambient. It was found that the nitrided oxide was more resistant to degradation in the SEG ambient than thermal and poly oxide; results reported here for the first time. The increased resistance of nitrided oxide in SEG ambient coupled with their superior performance as thin gate insulators makes them an excellent candidate for use in novel 3-D structures using selective silicon growth.

I. INTRODUCTION

SILICON Selective Epitaxial Growth (SEG), Epitaxial Lateral Overgrowth (ELO), and Confined Lateral Selective Epitaxial Growth (CLSEG) have been identified as a key technology for the next generation VLSI/ULSI used to fabricate novel bipolar, MOS, BiCMOS, and SOI devices [1]–[4]. An important limitation in selective silicon growth is the degradation of thin masking oxide when placed in the growth ambient [5]. These novel 3-D devices require the use of thinner insulators which are resistant to degradation in selective growth ambient. In addition, recent advances in MIS sub-micron device fabrication technology have brought about device miniaturization to an extent that high quality and thin (~ 100 – 500 Å) gate insulators will be required for future scaled VLSI/ULSI devices. Recently, nitrided oxides have become of great interest as reliable dielectrics due to their increased dielectric strength and reduced degradation due to carrier injection [6], [7]. This letter reports the deteriorating effects of typical silicon SEG, ELO, and CLSEG ambient on nitrided oxide and three other insulators; namely, silicon dioxide, poly-oxide, and reoxidized nitride/oxide stack. The goal of the study was to determine which dielectric is most resistant to degradation during typical SEG, ELO, or CLSEG ambient.

Manuscript received Feb. 21, 1995.

R. Bashir is with Analog Process Technology Development, National Semiconductor, Santa Clara, CA 95051 USA.

S. Kim, N. Qadri, D. Jin, G. W. Neudeck, and J. P. Denton are with the School of Electrical Engineering, Purdue University, West Lafayette, IN 47907 USA.

G. Yeric, K. Wu, and A. Tasch are with the School of Electrical Engineering, University of Texas, Austin, TX 78712 USA.

IEEE Log Number 9413805.

II. EXPERIMENTAL

The four different structures prepared for the study are shown in Fig. 1. For Set I, all oxides were grown in a dry O_2 ambient except the 1425 Å thick oxide, which was grown in a wet O_2 ambient. Set II was prepared by depositing ≈ 100 Å thin LPCVD nitride layer on the desired thermal oxide layers. A dry oxidation step was then performed at 1000°C for 30 minutes. For Set III, phosphorus was diffused on the front and back of the wafer. Amorphous silicon was then deposited using LPCVD at 550°C using SiH_4 decomposition. SUPREM III simulations and sheet resistivity measurements were used to verify that the phosphorus will diffuse up into the poly-Si and dope it during the subsequent oxidations. Wafer set IV was prepared using LPCVD oxide deposited at 450°C , which was nitrided using rapid thermal annealing for one minute at 1000°C in N_2O . Then, a 850°C , 20 minute dry O_2 oxidation was performed.

SEG ambient stressing was performed in a LPCVD RF-heated pan-cake type reactor. H_2 was used as carrier gas, SiCl_2H_2 as the silicon source, and HCl was used to suppress the nucleation of poly-silicon and obtain selectivity. A five minute prebake in H_2 at a temperature of 970°C and pressure of 150 Torr was carried out. Then, HCl was introduced in the chamber for 30 seconds. H_2 and HCl were used to etch the native oxide from seed holes opened for SEG. The chamber pressure was then reduced to 40 Torr and SiCl_2H_2 was added in the reactor for 10 minutes. After SEG ambient stressing, control (unstressed) and stressed wafers were metallized using Al-1% Si alloy and patterned. The backside of each wafer was used to make a contact for electrical measurements. Breakdown electrical field of the MIS capacitors, E_{BR} , were calculated by dividing the measured breakdown voltage by the insulator thickness. The breakdown voltage was defined as the voltage where the current increased beyond 10 nA. 100 capacitors were measured on each wafer. The sizes of the capacitors measured were $140 \mu\text{m}^2$.

III. RESULTS AND DISCUSSION

To quantify the degradation of the insulators in the SEG ambient, the yield of capacitors for each set of wafers was calculated and compared with the yield of control wafer sets which were not placed in the epitaxial reactor. The average breakdown field, E_{avg} , and standard deviation σ_E was calculated assuming a Gaussian distribution of the measured

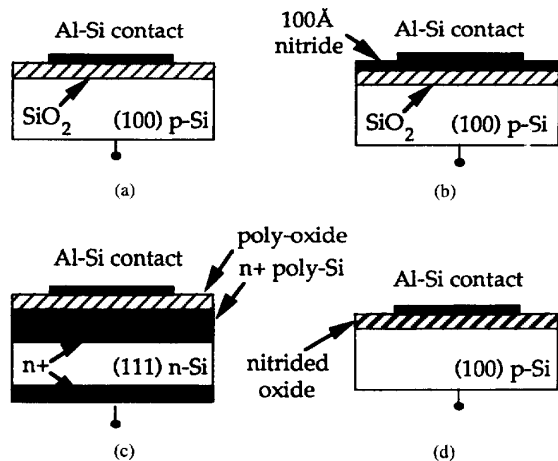


Fig. 1. Cross-sectional structure of the capacitors. (a) Thermal oxide (Set I), (b) Nitride/oxide (Set II), (c) Polyoxyde (Set III), and (d) Nitrided oxide (Set IV).

data for each set using all the thicknesses. Yield of tested capacitors was calculated by the following equation:

$$Y = \frac{\# \text{ of good capacitors}}{\# \text{ of capacitors}} \times 100. \quad (1)$$

The number of good capacitors was determined by the number of capacitors which have breakdown electric field larger than or equal to one standard deviation less than the average breakdown electric field for the entire set:

$$\# \text{ of good capacitors} = \text{capacitors with } E_{BR} \geq E_{avg}(\text{set}) - \sigma_E(\text{set}). \quad (2)$$

Fig. 2(a)–(d) shows the yield as a function of dielectric thickness for each insulator type before and after the SEG ambient stressing. Fig. 2(a) shows that, after SEG ambient stressing, the thin thermal oxides have degraded excessively. These results confirm the conclusions of an earlier study [5]. Fig. 2(b) shows that silicon nitride is very resistant to degradation in the SEG ambient. The apparent increase in the yield in Fig. 2(b) can be attributed to statistical fluctuations and processing conditions of the control set. Fig. 2(c) shows that, similar to the thermal oxide, the thinner poly oxides have been degraded. Fig. 2(d) shows that the nitrided oxides can withstand the SEG ambient conditions better than the thermal oxide and poly-oxide. The yield for the capacitors with thinner oxides is significantly higher than the respective thermal and poly-oxides. Thus, nitrided oxide could be a very useful insulator for 3-D devices due to its increased resistance against SEG ambient conditions and improved properties as a thin gate dielectric.

The result that nitride/oxide stack was most resistant to degradation can be explained by the fact that silicon has a higher absorption energy of nucleation on Si₃N₄ than on SiO₂ [8]. Silicon does react with the masking oxide according to the reaction in (3) for sufficiently low partial pressures of H₂O and O₂:

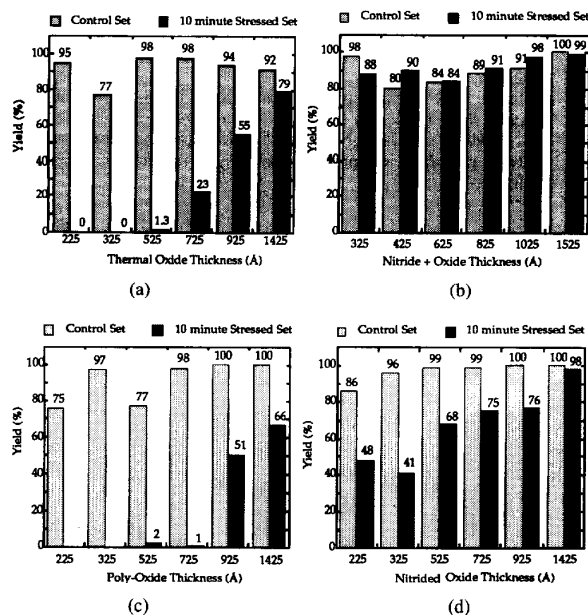
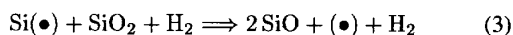


Fig. 2. (a) Yield for the various thermal oxide thicknesses for the control and stressed sets, (b) yield for the various nitride/oxide stack thicknesses for the control and stressed sets, (c) yield for the various poly-oxide thicknesses for the control and stressed sets, and (d) yield for the various nitrided oxide thicknesses for the control and stressed sets.

where (\bullet) is a surface site. The reaction of silicon with silicon nitride, however, is not clear. Our results confirm that, under the same conditions, silicon does not react as readily with Si₃N₄ as with SiO₂ [8]. It can be postulated that the increased resistance of the nitrided oxide insulator is directly related to the nitrogen content in the film.

IV. CONCLUSIONS

The important result that nitrided oxides can withstand the SEG ambient better than thermal or poly oxide has not been reported before. The reoxidized nitride/oxide stack was the most resistant to the SEG ambient, though not useful as a gate insulator. The increased resistance of the nitrided oxides in SEG ambient coupled with their superior performance as thin gate insulators makes them an excellent candidate for use in novel 3-D structures using selective silicon growth. In addition, a reduced degradation directly corresponds to reduced surface roughness and decreased thermal stress induced defects.

ACKNOWLEDGMENT

The authors thank S. Venkatesan for helpful discussions.

REFERENCES

- [1] G. W. Neudeck *et al.*, "Three dimensional devices fabricated by silicon epitaxial lateral overgrowth," *J. Electron. Materials*, vol. 19, no. 10, p. 1111, 1990.
- [2] L. Jastrzebski, "SOI by CVD: Epitaxial lateral overgrowth process—Review," *J. Crystal Growth*, vol. 63, p. 493, 1983.

- [3] R. Bashir, S. Venkatesan, G. W. Neudeck, and J. P. Denton, "A poly-silicon contacted sub-collector BJT for a 3-dimensional BiCMOS process," *IEEE Electron Device Lett.*, vol. 13, no. 8, p. 392, Aug. 1992.
- [4] A. Tasch, "Hot carrier suppressed sub-micron MOSFET device," *SRC Contract Rev.*, University of Texas, Austin, 1991, p. 28.
- [5] J. A. Friedrich and G. W. Neudeck, "Oxide degradation during selective epitaxial growth of silicon," *J. Appl. Phys.*, vol. 64, no. 7, p. 3538, 1988.
- [6] M. M. Moslehi and K. C. Saraswat, "Thermal nitridation of Si and SiO₂ for VLSI," *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, p. 106, Feb. 1985.
- [7] J. Ahn and D. L. Kwong, "Electrical properties of MOSFET's with N₂O-nitrided LPCVD SiO₂ gate dielectrics," *IEEE Electron Device Lett.*, vol. 13, no. 9, p. 494, Sept. 1992.
- [8] W. A. P. Claassen and J. Bloem, "The nucleation of CVD silicon on SiO₂ and Si₃N₄ substrate, II. The SiH₂Cl₂-H₂-N₂ system," *J. Electrochemical Soc.*, p. 1836, Aug. 1980.