Characterization of sidewall defects in selective epitaxial growth of silicon

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The sidewall defects in high quality selective epitaxial growth (SEG) of silicon were characterized. Three different SEG diode structures were fabricated and the bulk and perimeter defects were characterized through electrical measurements and transmission electron microscopy (TEM). The structures investigated were SEG grown in a 1.2 μm thick wet-etched field oxide, SEG grown in 1.2 μm thick reactive-ion etched field oxide, and SEG grown in a 1.2 μm high and 0.3 μm wide sidewall oxide cavity. The thin sidewall oxide cavity SEG diode showed the best ideality factors and minimum saturation current densities for diodes intersecting the sidewall, indicating the least thermal stress generated at the SEG/oxide sidewall interface during the cool-down period. Cross-sectional TEM micrographs showed no defects in the bulk SEG or at the sidewall, indicating that the thermal stress in all the processes was not high enough to cause plastic deformation, dislocations, or stacking faults.

I. INTRODUCTION

Selective epitaxial growth (SEG) of silicon has been identified as a key technology for the next generation very large scale integrated/ultralarge scale integrated circuits (VLSI/ULSI) which will use novel three-dimensional bipolar, metal oxide semiconductor, bipolar-complementary metal oxide semiconductor, and silicon-on-insulator (MOS, BiCMOS, and SOI) devices.[1,2] SEG and related selective growth techniques such as epitaxial lateral overgrowth (ELO) and confined lateral selective epitaxial growth (CLSEG) have been used to fabricate novel three-dimensional devices.[3–7] (See Fig. 1.) The bulk SEG silicon material is of excellent quality but the material close to the sidewall insulator can have a high defect density. Various authors have reported the presence of defects along the sidewall.[8–10] A factor of 10–100 increase in leakage currents has been reported when the junctions intersect the SEG sidewall. The presence of the sidewall defect is considered to be the single most important problem hindering the widespread use of SEG in semiconductor processing because junctions and depletion regions intersecting these sidewall defects will result in undesirable recombination–generation currents. Hence, it is extremely important that these defects need to be characterized and eliminated.

It is postulated that the main cause of the SEG/ELO sidewall defects is thermal stress after the SEG growth during the cool-down period.[2,9,10] The oxide /silicon interface is a location of high internal strain. As a strain relief mechanism, stacking faults could be generated in the silicon material. The strain could be introduced as a result of the difference in thermal coefficient of expansion between the silicon overgrowth and the oxide. At high temperatures, the silicon yield strength is lowered and the thermal stress could exceed the material yield strength. If this situation occurs, the internal stress will be relieved by plastic deformation of silicon.[10,11] Some practical steps have been suggested to reduce the internal strain introduced by the Si overgrowth.[10] The insulating film could be made thinner, which would reduce the internal strain. The thermal stress could also be reduced if the thermal coefficient of expansion of the insulator next to the overgrowth is matched to that of silicon. However, the very limited choices of insulator do not allow the matching of expansion coefficients. The reduction in growth temperature itself should reduce the stress and strain developed in the material, at the expense of slower growth rates.

It is the purpose of this paper to characterize the sidewall defects in selective epitaxial growth of silicon. By the fabrication of a unique structure, it is shown that the quality of the SEG/oxide sidewall interface can be greatly improved by using a thin sidewall oxide. The results are attributed to a lower thermal stress in the thin sidewall oxide cavity SEG structure. The material quality was electrically characterized by fabricating diodes using selective epitaxial growth and chemical-mechanical polishing with junctions intersecting the sidewall interface of interest. Bulk and perimeter ideality factors and saturation current densities were extracted to characterize the bulk and sidewall SEG material.

II. CHARACTERIZATION TECHNIQUE

The current through a diode in the forward bias region is the sum of a diffusion component and a recombination current. The recombination current is characterized by the ideality factor η, theoretically equal to 2. The recombination current is dominant at low forward biased applied voltages while the diffusion current dominates at higher voltages. The

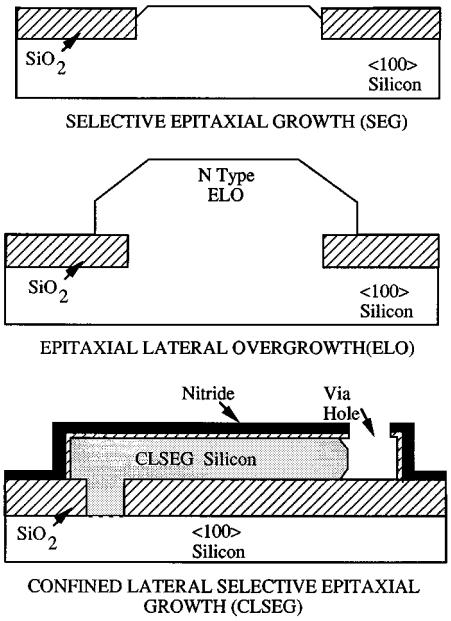

FIG. 1. Various selective silicon growth techniques.

diffusion and recombination current can be lumped together, and the perimeter current component can be included to obtain the total diode current:

$$I = AJ_{b0}\left[\exp\left(\frac{qV}{\eta_b kT}\right)-1\right]+PJ_{p0}\left[\exp\left(\frac{qV}{\eta_p kT}\right)-1\right]. \quad (1)$$

In Eq. (1), A is the diode area, J_{b0} is the bulk saturation current density (in A/cm^2), η_b is the bulk ideality factor, P is the perimeter of the diode, J_{p0} is the perimeter saturation current density (in A/cm), η_p is the perimeter ideality factor, and V is the applied voltage. Dividing the resultant equation by the area results in the following:

$$J = J_{b0}\left[\exp\left(\frac{qV}{\eta_b kT}\right)-1\right]+\frac{P}{A}J_{p0}\left[\exp\left(\frac{qV}{\eta_p kT}\right)-1\right]. \quad (2)$$

Thus, for a given voltage, if the measured current density is plotted as function of the perimeter to area ratio, a straight line should be obtained with the slope given by the perimeter current component and the x intercept given by the bulk current component. If the measurement is performed at two different voltages between which the ideality factor is assumed to be constant, then two values of slopes can be obtained as shown in the following:

$$\text{slope } 1 = J_{p0}\left[\exp\left(\frac{qV_1}{\eta_p kT}\right)-1\right], \quad (3)$$

$$\text{slope } 2 = J_{p0}\left[\exp\left(\frac{qV_2}{\eta_p kT}\right)-1\right]. \quad (4)$$

The above two equations can be solved simultaneously to obtain the values of J_{p0} and η_p. This technique has been applied on GaAs diodes and solar cells to study the effect of perimeter recombination.[12] The bulk current components can be obtained by dividing Eq. (1) by the perimeter to obtain

$$\frac{I}{P} = \frac{A}{P}J_{b0}\left[\exp\left(\frac{qV}{\eta_b kT}\right)-1\right]+J_{p0}\left[\exp\left(\frac{qV}{\eta_p kT}\right)-1\right]. \quad (5)$$

Thus the bulk current components can be obtained from the slope of the least-squares fit of an I/P vs A/P plot. Taking the data at two different voltages allows for the extraction of J_{b0} and η_b, which characterize the bulk current component.

III. DEVICE FABRICATION

Five different p^+/n diode structures were fabricated in this study. Two were used as a reference and the other three were the SEG diodes under investigation.

A. Process 1

The first reference diode (process 1) was a conventional recessed local oxidation of silicon (LOCOS) isolation sidewall oxide diode in n-type, 1–5 Ω cm, {100} substrate. A photoresist mask was used to etch through a nitride, pad oxide, and 0.5 μm of silicon using reactive ion etching (RIE). The 0.8 μm LOCOS oxide was then grown, the nitride and pad oxide removed, and the wafer front was implanted with boron to form the p^+ diode and the wafer back was implanted with arsenic to form the back contact. The implants were activated by a 1000 °C wet oxidation resulting in 0.12 μm oxide on the diode. Contacts were opened and devices were metalized with approximately 0.25 μm of Al–1% Si alloy which was defined using lift-off. The wafers were annealed at 415 °C in dry N_2 for 20 min. The final cross section of the two reference diodes is shown in Fig. 2(a).

B. Process 2

This diode structure also served as a reference. The fabrication process started with n-type, 1–5 Ω cm, {100} silicon wafers. Boron was implanted in the entire front for p^+ diode formation and the back of the wafer was implanted with arsenic. A photoresist mask was then used to anisotropically etch through 2 μm of silicon using Freon 115 gas. The implants were activated and contacts were formed similar to the diode of process 1. The final cross section is shown in Fig. 2(b). Using process 2, the reactive-ion-etched sidewall can be examined and can be compared with the LOCOS and other SEG sidewall diodes.

C. Process 3

Process 3 was a diode structure with the SEG oxide sidewall interface of interest. The fabrication process started with n-type 1–5 Ω cm, {100} silicon wafers. The device structures were oriented along the ⟨100⟩ direction on the {100} plane to reduce perimeter defects and enhance the material quality. The process began by growing a 1.2 μm of field oxide on the silicon. A positive photoresist mask was then used to wet etch the oxide. SEG/ELO of silicon was performed in a reduced-pressure pancake-type rf-heated epitaxial reactor. A 5 min hydrogen bake and 30 s HCl etch, both at 970 °C, were used prior to growth. SEG/ELO was then started from the silicon seed holes at 970 °C and 40 Torr at a growth rate of ≈0.10 μm/min to result in 2.5 μm of growth. The growth

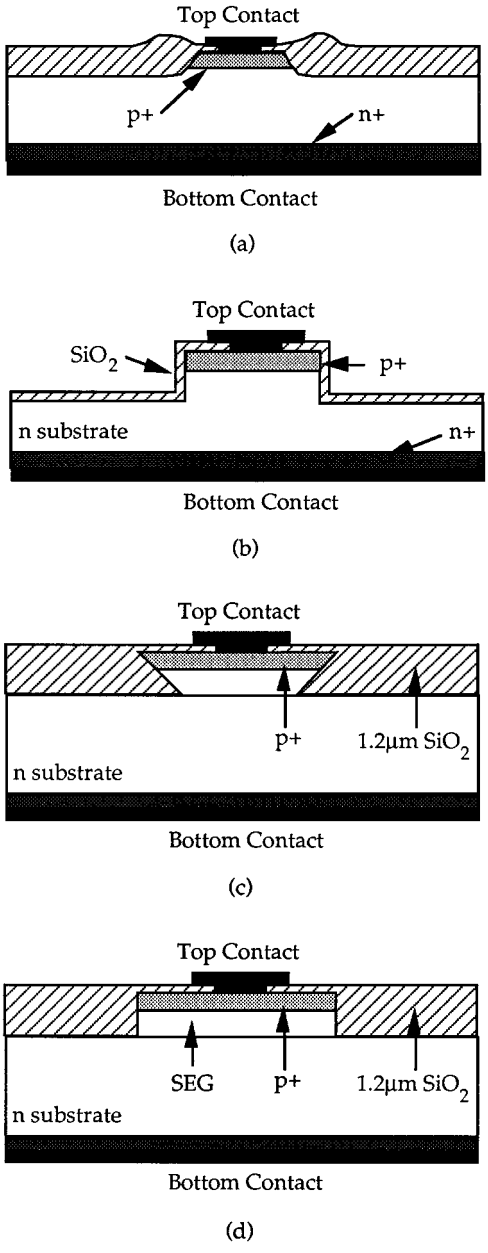

FIG. 2. The two reference diode structures. (a) Recessed LOCOS isolated diode structure, process 1, (b) RIE sidewall diode, process 2, (c) wet-etched oxide SEG diode, process 3, (d) RIE oxide SEG diode, process 4.

did result in silicon material over the field oxide. The wafer was chemical-mechanically polished (CMP) down to the top surface using the field oxide as an etch stop. All of the overgrowth was removed and a planar surface was obtained. After the CMP, a p^+ diode was formed and the fabrication proceeded exactly as in processes 1 and 2. The final cross section of the diode is shown in Fig. 2(c).

D. Process 4

Process 4 was a diode structure fabricated identical to that of process 3 except that fact that the oxide was anisotropically RIE using CHF_3 and O_2. A dry oxidation at 1000 °C for 20 min was performed to anneal the RIE damage. The resultant oxide was etched using BHF (buffered hydroflouric

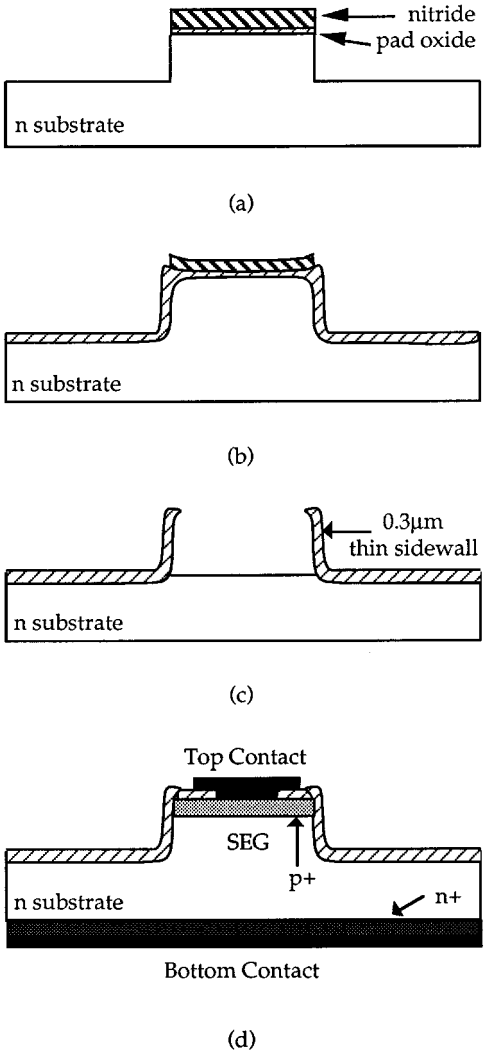

FIG. 3. Process flow of the thin oxide cavity SEG diode, process 5.

acid). The rest of the processing including the SEG was identical to the earlier process. The structure of process 4 is also an ideal candidate for a facet-free isolation technology using SEG and chemical-mechanical polishing.[13,14] The final cross section of the diode is shown in Fig. 2(d).

E. Process 5

Process 5 consisted of a unique structure having only a 0.3 μm oxide sidewall before the SEG was performed. The motive behind fabricating this process was to examine the effect of sidewall oxide thickness before the SEG. The fabrication process started with n-type, 1–5 Ω cm, {100} silicon wafers. The device structures were oriented along the $\langle 100 \rangle$ direction on the {100} plane to reduce perimeter defects and enhance the material quality. The process began by growing an 800 Å thick pad oxide followed by a 0.25 μm Si_3N_4 deposition at 800 °C. A photoresist mask was used to anisotropically etch through the Si_3N_4 in a RIE using SF_6. The oxide was then etched using Freon 115. Following the oxide etch, 1 μm of the silicon was anisotropically etched in Freon 115 plasma as shown in Fig. 3(a). The photoresist mask was then removed and the wafers were oxidized at 1050 °C to

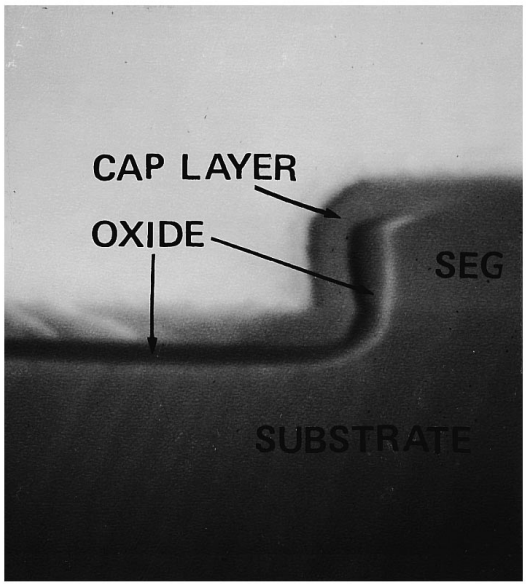

FIG. 4. SEM showing the final cross section of the thin oxide cavity SEG diode.

form an oxide 0.5 μm thick, as shown in Fig. 3(b). The nitride and pad oxide were then removed during which the oxide on the substrate was reduced to 0.30 μm. The silicon in the active areas was now exposed. The single crystal silicon was etched down to the substrate level using a mixture of 47 g KOH, 127 ml H_2O, and 39 ml isopropanol. Next, SEG was performed similar to the last two processes. Silicon did not grow out and over the thin oxide and the planarization step was not used. Following the SEG, the diode formation was the same as described for the previous diodes. The final cross section is shown in Fig. 3(d). The thin oxide wall is about 1.2 μm high and 0.3 μm wide as shown in the cross-sectional SEM in Fig. 4. SEG was grown in the region bounded by the thin sidewall.

IV. CHARACTERIZATION RESULTS

The electrical characterization of the sidewall and bulk was performed by the method described earlier. The current through the diode was measured at three different voltages of 0.425, 0.45, and 0.475 V, where the ideality factor was constant. The measured current was divided by the area and the current density obtained was plotted versus the P/A ratio. The least-squares fit of the data was used to obtain the sidewall parameters η_p and J_{p0}. Figure 5 shows one representative J vs P/A plot. To obtain the bulk parameters η_b and J_{b0} for the diodes, I/P was plotted as a function of A/P. The bulk parameters will include the contribution from all defects except the ones at the sidewall interface. Twenty devices are measured and the average values of parameters are listed in Table I.

Process 1 shows excellent bulk and sidewall parameters indicating almost no recombination in the silicon-controlled rectifier (SCR) region. Process 2 diodes show an ideality factor of 1.1 which could be due to the presence of RIE damage along the sidewall not completely removed by the oxidation. The sidewall ideality factor is slightly higher than

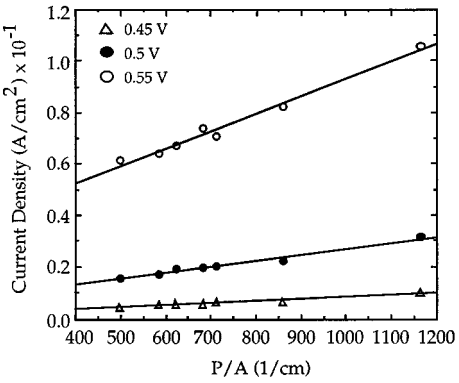

FIG. 5. A representative current density vs perimeter to area ratio plot.

the LOCOS and indicates a lower quality sidewall. The reverse leakage was measured so that the depletion region would not go into the substrate. Process 3 shows a higher ideality factor of 1.37 for the sidewall and 1.32 for the bulk. This indicates the presence of defects along and close to the SEG sidewall. The ideality factor at 0.45 V for processes 3 and 4, 1.29 and 1.23, respectively, are very close; however, the perimeter and bulk parameters are different. The RIE perimeter values are higher than the wet-etched oxide process. This could be due to that rough oxide sidewall due to the RIE.

The thin oxide cavity SEG diode (process 5) showed the most interesting results. The ideality factors were close to the values of processes 1 and 2 even though they had the selective epitaxial growth sidewall interface. The low ideality factors can be attributed to the thin sidewall oxide. If the defects are generated due to thermal stress during the cool-down period after the SEG growth, then the SEG Si grown in this structure will experience the minimum thermal stress due to the presence of the thin oxide which is free to expand and contract. Also, the corner of the substrate/SEG intersection will experience the least thermal stress due to the thin oxide present there.

Transmission electron microscopy was also performed on the three SEG diodes, from processes 3, 4, and 5, to examine the sidewall defects on samples which were not planarized. No defects were observed in the samples close to the sidewall and bulk. If the thermal stress is the main cause of the SEG sidewall defects, then the SEG in these diodes can be

TABLE I. Summary of results.

Device	η at 0.45	η_p	J_{p0} (A/cm)	η_b	J_{b0} (A/cm^2)	J_{rev} (A/cm^2)
Sample 1 (LOCOS)	1.02	1.00	4.35×10^{-14}	1.05	4.04×10^{-11}	2.31×10^{-7} at -2 V
Sample 2 (RIE substrate)	1.10	1.15	8.05×10^{-13}	1.05	8.21×10^{-11}	2.03×10^{-7} at -2 V
Sample 3 (wet-etch oxide)	1.29	1.37	1.56×10^{-11}	1.32	6.78×10^{-9}	2.88×10^{-7} at -1 V
Sample 4 (RIE oxide)	1.23	1.49	4.17×10^{-11}	1.09	3.59×10^{-10}	4.00×10^{-7} at -1 V
Sample 5 (thin oxide wall)	1.15	1.21	3.79×10^{-12}	1.08	1.91×10^{-10}	4.97×10^{-7} at -1 V

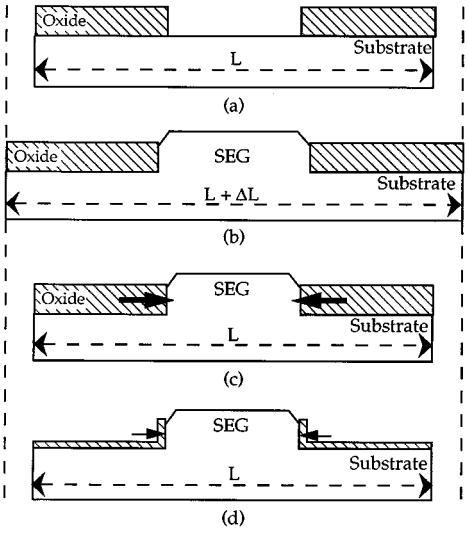

FIG. 6. Schematic showing the compressive forces on the SEG sidewall during the cool-down period, (a) before the SEG, (b) after the SEG with the wafer in the expanded state, (c) after the cool-down period, (d) the thin oxide sidewall cavity wafer after the cool-down period.

postulated to be strained but not enough to cause plastic deformation resulting in dislocations. The thermal stress and strain could cause traps in the energy gap, resulting in a higher recombination and hence a slightly higher ideality factor but not enough to cause plastic deformation.

V. DISCUSSION

The results described above can be explained by taking into account the thermal stress generated at the SEG sidewall. As the temperature is ramped up before the growth, there is an increase in the volume of the oxide and the silicon substrate according to their respective coefficients of thermal expansion, α, which is a function of temperature. At 970 °C, α_{Si} and α_{ox} are approximately $3.9\times10^{-6}/$ °C and $0.5\times10^{-6}/$ °C, respectively. The silicon substrate plays a very important role in determining the stress at the SEG sidewall. It will expand more in the horizontal direction than along its thickness and about 5–8 times more than the oxide. SEG Si is grown at the high temperature, when the substrate is in the expanded state. During the cool-down period the substrate will contract back and force the oxide, which is bonded to the substrate, to apply a compressive stress on the SEG. As shown in Fig. 6, for processes 3 and 4 the entire field oxide is being contracted along with the substrate, whereas, for process 5, the oxide exerting the force is only 0.3 μm wide. The stress applied is not large enough to cause plastic deformation in all three structures.

VI. CONCLUSIONS

This article presented an extensive characterization of the sidewall defects in high quality selective epitaxial growth (SEG) of silicon with an oxide sidewall. The unusual interface of SEG with the sidewall oxide is prone to defects, the major cause being thermal stress generated in the cool-down period after the SEG. The experiments in this study proved that the sidewall oxide width, determining the thermal stress, plays a major role in determining the SEG sidewall material quality. Diodes were fabricated and electrically characterized to show that the thin oxide cavity SEG diode (process 5) exhibited the lowest ideality factors and saturation current density as compared to thick oxide cavity SEG diodes (Processes 3 and 4). A lower growth temperature would further reduce the thermal stress and improve the sidewall SEG material quality.

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