BRIEF REPORTS AND COMMENTS

Doping of polycrystalline silicon films using an arsenic spin-on-glass source and surface smoothness

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In this brief, the doping of polycrystalline silicon from a commercially available arsenic spin-on glass (SOG) source is described for the first time. It is shown that the arsenic SOG source provides low sheet resistivities in thin polycrystalline silicon films which can be used as gates and contacts. In addition, the polycrystalline silicon films doped with arsenic SOG and exposed to an oxidation step exhibit reduced top surface roughness when compared to films doped with phosphorus from a $POCl_3$ source. The minimization of the top surface roughness of the polyoxide is important for its use as a gate insulator in advanced three-dimensional complementary metal–oxide–semiconductor (CMOS) and as a sidewall contact in BiCMOS bipolar junction transistor devices.

I. INTRODUCTION

The use of spin-on–glass (SOG) as a dopant diffusion source has become more prevalent in recent years in the semiconductor industry. The motives behind its increasing use stem from its process-related advantages, reduced cost, and safety considerations.[1,2] The SOG source is an organic solution which can be applied on the wafer using standard photoresist equipment. Following a pyrolysis treatment, the solution produces a doped silicate film which is then used as the impurity diffusion source. The process related advantages include the possibility of obtaining varying sheet resistivities by only changing the film thickness while keeping the furnace conditions fixed. In addition, the use of a SOG source makes the process safer because of the small amount of dopant handled per wafer and the use of non-gaseous sources.

Polycrystalline silicon films are frequently used in the semiconductor industry as metal–oxide–semiconductor (MOS) transistor gates, bipolar transistor emitters and base contacts, and for interconnects. The grain size and the surface texture of these films are a function of the polysilicon deposition and doping conditions as well as subsequent oxidations and thermal cycles.[3,4] The top surface of the oxide grown on these polycrystalline silicon films is the

subject of this brief. The top surface roughness of the polysilicon might not be important for conventional devices; however, it is of great importance in advanced three-dimensional (3D) complementary MOS (CMOS), BiCMOS,[5,6] and for multilevel dielectrics. In these 3D devices, selective epitaxial growth (SEG), and epitaxial lateral overgrowth (ELO) are used to grow single crystal silicon on top of existing polysilicon gates protected by a thermal polyoxide. It is necessary to minimize the roughness of the polysilicon top surface and hence the roughness of the polyoxide when ELO silicon is grown on top of the structure to serve as a second MOSFET. In this 3D CMOS structure the shared gate is sandwiched between the n-MOS and p-MOS devices. The interface must be smooth in order to reduce the carrier scattering and interface state density, as well as the potential defect generation in the ELO silicon.

It is the purpose of this brief to report sheet resistivities of polycrystalline silicon films doped with an arsenic SOG and to demonstrate that this type of doping, followed by oxidization, results in reduced surface roughness compared to conventional doping and oxidation techniques. Transmission electron microscopy (TEM) was used to examine the surface roughness for comparison of films doped with the arsenic SOG to those doped by phosphorus diffusion from $POCl_3$ and by arsenic implantation.

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TABLE I. Summary of process and measured parameters for the arsenic SOG dopant.

Run No.	Poly thickness (μm)	Spin speed (rpm)	Diffusion time (min)	Diffusion temp. (°C)	N_2 flow (sccm)	O_2 flow (sccm)	R_s ($\Omega/\square$)
1	0.35	3000	30	1000	2.5	0.5	$> 10^4$
2	0.35	3000	60	1000	2.5	0.5	2400
3	0.35	3000	60	1050	2.5	0.5	1850
4	0.35	3000	120	1100	2.5	0.5	535
5	0.60	2000	60	1100	2.5	0.0	1280
6	0.60	2000	60	1100	2.5	0.5	100
7	0.60	1500	120	1100	2.5	0.5	55
8	0.40	1000	60	1100	2.5	0.5	75

II. DOPING EXPERIMENTS/RESULTS

The arsenic SOG used in the this work was As-354 from Filmtronics, Inc.,[7] which produced layers with an arsenic concentration of 5×10^{20} cm^{-3}. Two inch silicon wafers were oxidized to form ~5000 Å of oxide. Following the oxidation, amorphous silicon was deposited in a low-pressure chemical vapor deposition (LPCVD) system using the decomposition of silane at 550 °C at 120 mTorr. (It is known that the silicon deposited at 550 °C is amorphous, while the silicon deposited at higher temperatures is polycrystalline in structure.[3] Even the amorphous silicon changes into polycrystalline if it is exposed to a high temperature anneal or oxidation. In this brief, the film before the high temperature step is referred to as "amorphous" while the film after the high temperature step is referred to as "polycrystalline." The film deposited at 550 °C is known to be smoother than the film deposited at higher temperatures and that is why the films used in this study were all deposited at 550 °C.) The SOG procedure commenced by performing a Pirhana clean using 1:2 H_2O_2:H_2SO_4 solution followed by a de-ionized rinse. Wafers were then baked at 150 °C to remove any residual moisture. The arsenic SOG was then spun on the wafer using a photoresist spinner. About 1 cm^3 of the solution was applied to the wafer and spun at different speeds for 15 s. The wafers were then baked at 150 °C for 15 min to remove the excess solvent in the film and to eliminate its hygroscopic properties so that it would not be sensitive to humidity. Next a high temperature diffusion step was used to drive the arsenic into the polysilicon film from the SOG. The diffusion was performed in a furnace tube in a nitrogen and/or oxygen ambient. All the diffusion steps included a 3 min push and pull in pure nitrogen. After the thermal diffusion, the wafers were allowed to cool to room temperature before the SOG film was etched off in a buffered oxide etch. The SOG film could not be etched consistently and repeatably unless the wafer was cooled to room temperature. The sheet resistivities of the polysilicon film were then measured using a four-point probe apparatus.

Table I lists the sheet resistivities resulting from different experiments. Eight different runs were performed with varying diffusion times, temperatures, and application spin speeds. The sheet resistivity of the poly-Si film decreased as the diffusion temperature increased and as the diffusion time was increased. The sheet resistivity also decreased as the spin speed was decreased. A smaller speed results in a thicker film and hence provides more arsenic for diffusion.

The oxygen content in the ambient is also a vital factor in determining the sheet resistivity. It has been reported that increasing the oxygen content monotonically will decrease the sheet resistivity until a minimum is reached.[8] Further increase in the oxygen content starts to increase the sheet resistivity. The initial decrease in the sheet resistivity is attributed to an enhanced arsenic diffusivity in the presence of oxygen. A further increase in oxygen initiates the growth of an oxide barrier at the silicon interface resulting in less incorporation of arsenic in the silicon.
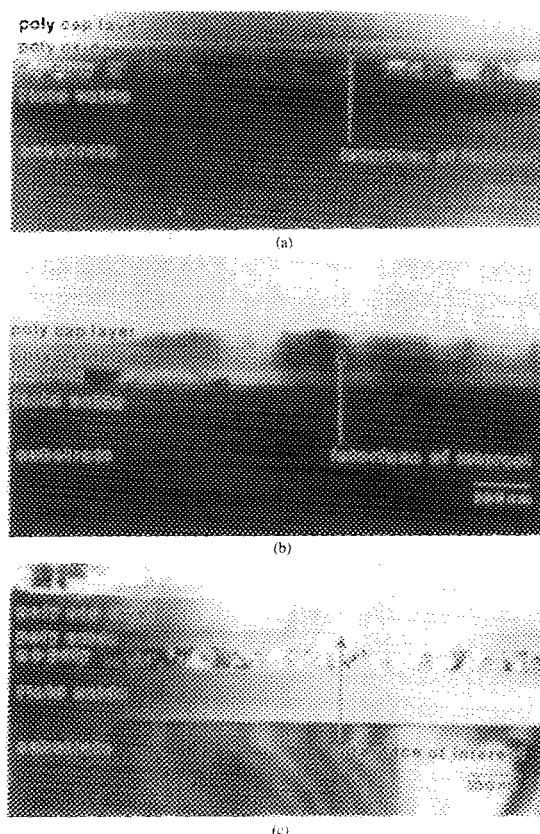

FIG. 1. TEM cross section of the three samples used for comparison of top oxide interface. (a) Sample A, arsenic SOG doped, (b) sample B, phosphorus gas doped, (c) sample C, arsenic implanted.

III. TEM STUDY/RESULTS

TEM was used to examine the surface roughness of the polycrystalline silicon films doped with the arsenic SOG. A comparison was performed between the following samples; sample A, which was a polycrystalline silicon film doped from arsenic SOG; sample B, a polycrystalline silicon film doped with phosphorus deposition in a furnace tube; and sample C, a polycrystalline silicon film doped with arsenic by ion implantation. Sample A was prepared as run No. 8 in Table I. Sample B was prepared by doping a 0.4 μm thick amorphous silicon film with gas-phase phosphorous for 15 min at 950 °C from a $POCl_3$ source. Sample C was doped by implanting a 0.4 μm thick amorphous silicon film with arsenic at an energy of 50 keV and to a total dose of 1×10^{16} cm^{-2}. All three samples were then oxidized at 1000 °C for 15 min in a wet oxidizing ambient. After the oxidation, the sheet resistivity of sample B was 15 $\Omega/\square$ and that of sample C was 65 $\Omega/\square$. Note that in Table I, run 7 at 1500 rpm, 120 min anneal at 1100 °C has a sheet resistance of 55 $\Omega/\square$, which is quite adequate in most cases for a MOS field effect transistor (MOSFET) gate.

A thick polycrystalline silicon cap layer was then deposited, solely to protect the oxide surface from damage during TEM sample preparation. The interface of the oxide/cap polylayer was the interface of most interest in this study. Figure 1 shows the TEM images of the three samples on the same magnification scale. As can be seen from the micrographs, the oxide surface of sample B is rough compared to the other two samples. Small protrusions on the oxide surface are clearly visible. The oxide surfaces of samples A and C are almost equally smooth and much improved over B. Sample A shows an acceptable amount of surface roughness. The TEM results were also substantiated by Nomarski imaging, which gave the same results. Increased roughness of the phosphorus-doped film could be attributed to the anisotropic oxidation rates of the different grains as compared to the arsenic-doped films.

IV. CONCLUSIONS

In this brief, it is shown that the arsenic SOG source can be used to obtain low sheet resistivities in thin polycrystalline silicon films. The polycrystalline silicon films doped with arsenic SOG and exposed to an oxidation step exhibit reduced top surface roughness when compared to films doped with phosphorus from a $POCl_3$ source and nearly equivalent roughness when compared to films doped by arsenic implantation.

ACKNOWLEDGMENT

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