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On the design and fabrication of novel lateral bipolar transistor in a deep-submicron technology ☆

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Abstract

The performance of a npn Lateral Bipolar Transistor (LBJT), based on a minimally modified submicron MOSFET without gate oxide, was studied by means of simulations and measurements on fabricated devices. Large-tilt angle, single-sided implants were successfully used to control the breakdown voltage by tailoring an asymmetric collector doping profile and providing a lightly doped region on the collector side to increase the breakdown voltage. This was accomplished by using a base/gate pedestal as the mask for the large-tilt angle, single sided implantation in a self-aligned fashion. The individual collector–base and emitter–base junctions were found to be of excellent quality but, as expected due to the lack of carrier confinement in the base of devices built on bulk silicon, the common emitter current gain was lower than one. Two options enhancing the device performance were studied using simulators: building the LBJT on Silicon-on-Insulator (SOI) or introducing SiGe into the base. The SOI device promises to provide better performance and ease of processing when compared to the SiGe base device.

Keywords: Lateral bipolar transistor; Silicon-on-insulator device; Submicron technology; Large-angle implant

1. Introduction

1.1. Motivation

Lateral bipolar transistors have been routinely used in CMOS processes for dc and low frequency analog circuits, like current mirrors and voltage references [1,2]. But their performance is severely limited by the parasitic transistors introduced by the isolation wells, and by the large volume and area of the base (which limit the frequency response). Their great advantage is that they can be incorporated into a CMOS integrated circuit (IC) with only very minor modifications to the process. The most common LBJTs are modified MOSFETs that preserve the gate electrode and add an ohmic contact to the base (channel) outside of the intrinsic base area [1–7]. While this approach provides the most compatibility with standard CMOS processes, it may result in high base resistance and increased area. Thus, it is desirable to establish a polysilicon contact all along the base, as has been described in several reports [8–14]. It is also necessary to create a lightly doped region on the collector side to increase the breakdown voltage. The drawback of many of these devices is that they deviate substantially from the standard CMOS process in order to establish the base contact and/or the lightly doped collector region.

As CMOS technology approaches the sub-0.1 μm regime the fabrication process complexity increases, the design becomes progressively more difficult, performance is more sensitive to process fluctuations and the reliability suffers, specially that of the gate oxide which has reached a thickness on the order of 30 Å or less. In the limit when the oxide thickness is zero and the gate is shorted to the channel, the MOS device becomes a Lateral Bipolar Junction Transistor (LBJT). The source, drain, and gate electrodes of the MOSFET being equivalent to the emitter, collector and base terminals of the LBJT, respectively. With future fabrication techniques, the base width of the LBJT (equivalent to the channel length of the MOSFET) could be of the same order of magnitude as that of modern vertical bipolar transistors (~200 Å). This device could theoretically be a good alternative to MOSFETs since, for extremely thin gate oxides, their gate leakage current could become comparable to the base current of a LBJT, with the advantage that reliability might be improved since there is no ultra-thin gate oxide. At the same time, the LBJT could offer a highly scalable and easy to manufacture bipolar transistors for BiCMOS circuits.

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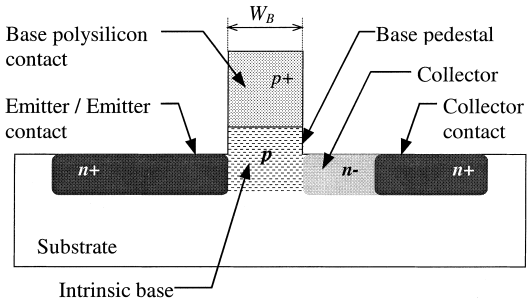

Fig. 1. Basic structure of the LBJT. The base pedestal is created because there is no gate oxide to act as an etch-stop during the polysilicon etch.

We present here a very simple approach to building LBJTs by making minimal modifications to a conventional MOSFET. The base contact is established by removing or inhibiting the growth of the gate oxide, and the collector is created in a self-aligned way by using large-tilt angle, single-sided implants. Fig. 1 shows the basic geometry of the LBJT, where the intrinsic base width is equivalent to the channel length of the MOSFET. Such a structure has a poor performance on bulk silicon, but it is ideally suited for fabrication on Silicon-on-Insulator (SOI) substrates, as will be shown in the following sections.

1.2. Overview of the device

Fig. 1 shows the basic geometry of the LBJT, where the intrinsic base width of the LBJT is equivalent to the gate length of the MOSFET. In the figure, the region indicated as being the base will be called throughout this document "intrinsic base" or just "base", when discussing the lateral device, while any other p type region directly shorted to the base will be called "extrinsic base". Similar devices have been reported in the literature [5,6,8,10], with those built using SOI technology showing the most promise for high frequency, low power BiCMOS circuits. In principle, the LBJT offers all the advantages of a bipolar transistor over a MOSFET: Better current drive, good matching, lower sensitivity to process fluctuations, "sub-threshold" slope close to the ideal 60 mV/dec, capable of operating at lower voltage swings, etc. At the same time, the LBJT has a low collector resistance (compared to a vertical device) because there is no need for a buried layer and its linkage to the surface.

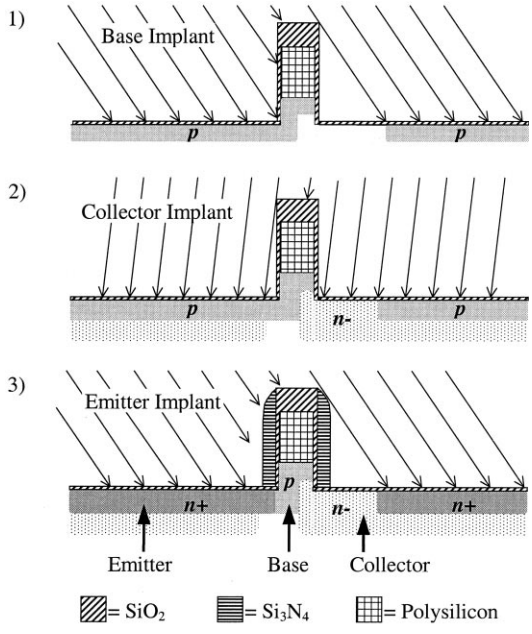

Fig. 2. Sequence of single-sided, large-angle implants used to create a self-aligned n− collector region, necessary for breakdown voltage control.

2. Fabrication

2.1. Base contact

As was said earlier, an ohmic contact between the gate polysilicon and the channel region (base) can be achieved by either removing from or inhibiting the growth of the gate oxide on the bipolar areas. Removing the oxide by directly masking it can introduce contamination and compromise its reliability. Thus, to avoid contamination, a thin protective layer of polysilicon can be deposited over the oxide immediately after its growth. The CMOS areas can then be masked while the polysilicon and gate the oxide are removed from the bipolar areas. Finally, the thick base/gate polysilicon layer can be deposited in the usual way.

An alternative approach could involve nitriding the silicon surface of the bipolar areas to retard the growth of the gate oxide on them [15–17]. However, this technique has not been tested to ensure that a low enough contact resistance is possible between the polysilicon and the oxidized–nitrided silicon.

2.2. Breakdown voltage control

To create a self-aligned, lightly-doped collector region necessary for controlling the breakdown voltage, we developed a method that takes advantage of single-sided, large-tilt angle implants. After the polysilicon is deposited, it is masked and implanted over the bipolar areas, then covered with an oxide layer that will shield it from subsequent implants, and annealed. Following this, the oxide/polysilicon stack is masked, etched and oxidized to form the base contact. Next, three large-angle implants dope the base, emitter and collector, as shown in Fig. 2. Base and collector implants are performed before the creation of the spacers, while the emitter is implanted after the spacers are in place. The oxide/polysilicon stack produces a shadow that keeps the emitter and base implants from reaching the n-collector region. The angles of the base and emitter implants, and the energy of the collector implant determine how much the collector n-region extends around the n+ implant. For a stack height of 4600 Å, an implantation

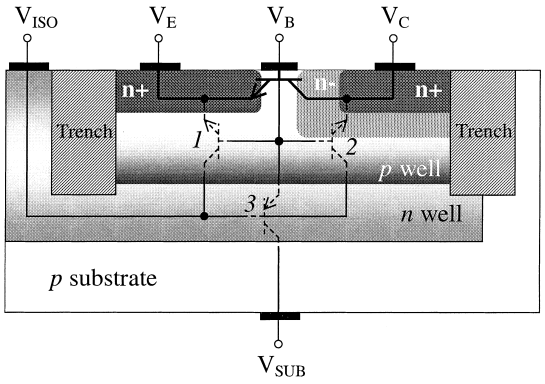

Fig. 3. Double well isolation structure with side-wall trenches. The intrinsic LBJT is shown with solid lines, and the three parasitic transistors that appear because of the isolation are indicated with dotted lines.

angle of 25° will result in a collector length of approximately 2100 Å.

Despite its simplicity, this method has some disadvantages. It requires all the LBJTs to be oriented in the same way, unless extra masks are used (although none of the extra masks will require critical alignment or small dimensions). And any topography on the wafer will create shadows that have to be taken into account during layout.

2.3. Device isolation

One of the problems in the fabrication of the lateral bipolar on bulk silicon, regardless of whether it is integrated with CMOS or not, is the creation of a structure that isolates the base of the device from the substrate. The isolation scheme studied is based on a double well that creates an n-type region between the base of the LBJT (p-well) and the substrate. The p-well is isolated from the substrate by applying a voltage to the n-well that reverse biases the junctions at each side of it (see Fig. 3). Consequently, the isolation voltage has to be the most positive one available in the circuit, since it has to be larger than the base and substrate voltages (the substrate is biased at the most negative voltage available). To avoid the parasitic transistors from causing large currents at the isolation bias terminal their gain has to be made as low as possible. This can be accomplished by making the p-well as deep and possible and with a high doping at its bottom, such that the Gummel number of the parasitic transistors becomes very high. But making the p-well very deep increases the charge storage and recombination in the base and the side wall capacitance. Consequently, the low parasitic current at the isolation terminal can only be achieved at the expense of switching time. It should be noted that the same problems apply to the fabrication of the NPN LBJT on a n-type substrate; the only difference being that the outer n-well is no longer necessary.

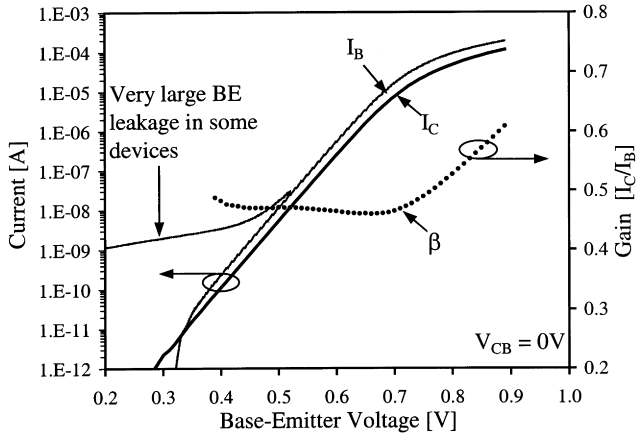

Fig. 4. Typical measured base current I_B, collector current I_C and common emitter current gain β, with collector and base shorted, for a device with a 0.25 μm drawn base width.

2.4. Process flow

A set of LBJTs were fabricated on 8″ wafers using a minimally modified, production-grade, 0.25 μm CMOS process and an existing set of CMOS test masks. This process converted all the properly oriented NMOS transistors in the mask set into NPN LBJTs. The main changes to the CMOS process were:

- No gate oxide is grown and the silicon surface is thoroughly cleaned to minimize the native oxide present before the deposition of the polysilicon layer.
- The polysilicon is blanket-implanted with boron (30 keV, 10^{16} cm^2) and annealed for 33 s at 900°C, immediately after deposition.
- A 1000 Å layer of SiO_2 is deposited over the polycrystalline silicon, after it is implanted, to shield it from subsequent implants.
- Single-sided, large-angle implants define the n+ emitter, n+ collector contact, and n− collector region, as depicted in Fig. 2. The n− region, with a peak doping on the order of 2×10^{17} cm^3, extends approximately 0.2 μm horizontally and 0.3 μm vertically beyond the n+ region.
- No silicide is formed to avoid shorting the n− and n+ regions on the collector side. This does degrades the quality of the contacts and increases the base resistance (the polysilicon is not silicided either). To preserve the silicidation, the n− collector region would have to be covered with oxide.

It should be noted that creating a custom isolation structure was not possible given the limitations imposed by the process used. The wafers had the standard CMOS well implants and LOCOS isolation. Consequently, the base of the transistors is shorted to the p-type substrate, which degraded the dc performance of the transistors and prevented the acquisition of ac measurements.

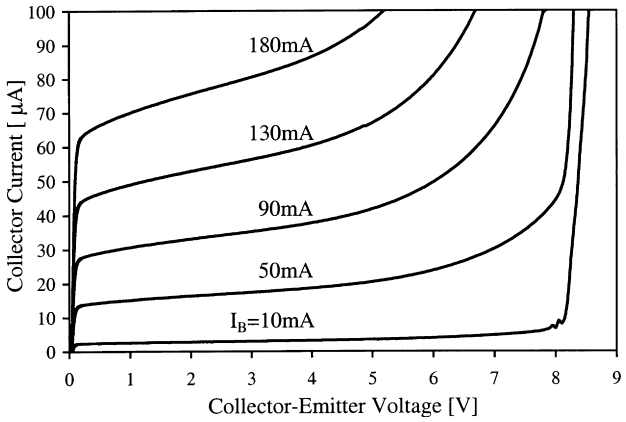

Fig. 5. Measured common emitter characteristics of a LBJT with a drawn base width of 0.21 μm.

3. DC electrical results

The fabricated devices were tested using an HP semiconductor parameter analyzer capable of performing picoampere current measurements. As expected, all of the fabricated LBJTs exhibit a common emitter current gain lower than one (see Fig. 4), primarily because of the lack of carrier confinement in the base. Despite the low gain, the devices display excellent common emitter characteristics, as demonstrated in Fig. 5. The quality of the individual junctions was also excellent as indicated by the results shown in Fig. 6. The C–B and E–B for junctions were ideal in the forward biased region with an ideality factor if 1.001 indicating that the damage due to the gate stack etch, the activation of the implants, and the multiple tilt angle implants was removed by the thermal cycling in the process. The E–B and C–B forward characteristics were also identical as expected. The reverse characteristics clearly show the improvement in leakage and breakdown in the C–B junction due to the presence of the n− region around the n+ collector region.

In order to study the causes for such a low gain, several simulations of the fabricated devices were performed using TSupremIV™ and Medici™. As shown in Fig. 7, most of the electrons travel from the emitter to the collector on paths that take them deep down into the substrate, where they are lost by recombination, resulting in a very low base transport efficiency. This occurs because electrons are emitted on all directions, but only those emitted within a certain solid angle will reach the collector.

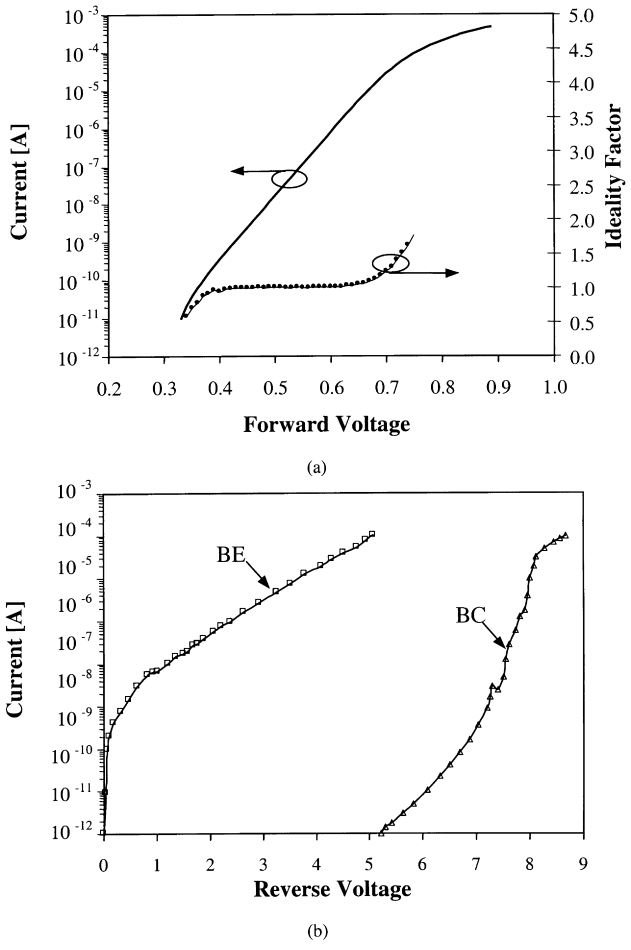

Fig. 6. Measured E–B and C–B junction characteristics: (a) forward *IV* curve and ideality factor; (b) reverse *IV* curves showing the improvement in CB breakdown with the n− implant.

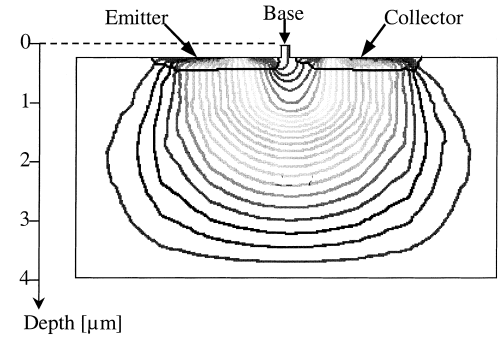

Fig. 7. Simulated current flow-lines in the fabricated devices, showing current injection deep into the substrate.

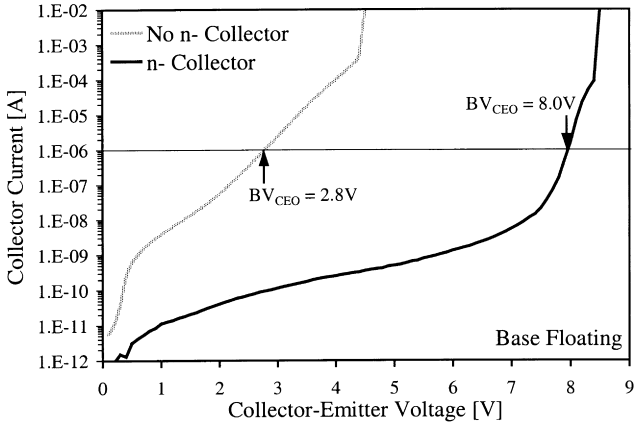

Fig. 8. Measured collector current as a function of collector–emitter voltage with the base floating, for a device with a 0.20 μm drawn base width.

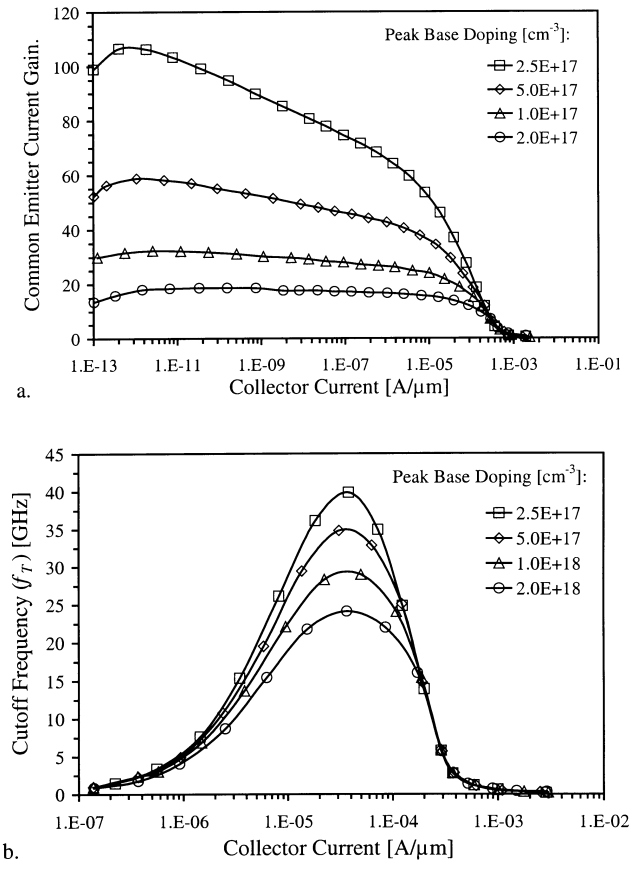

Fig. 9. (a) Common emitter current gain. (b) Cutoff frequency of a simulated SOI npn LBJT.

A clear indication of the effectiveness of the single-sided, large-angle implants for controlling the breakdown voltage is given by Fig. 8. These implants create a n − region with a peak doping on the order of 2×10^{17} cm^3, extending approximately 0.2 μm horizontally and 0.3 μm vertically beyond the n+ implant. Transistors with this region have a collector–emitter breakdown voltage of 8.0 V (defined at 1 μA) with the base open (BV_{CEO}), while those without it reach breakdown at 2.8 V. According to simulations, breakdown occurs at the collector-side corner of the base pedestal, but this could be an artifact caused by the particular shape of the corner produced by the process simulator. The maximum electric field can in principle occur at any point along the collector–base junction (this is why it is so important to have the n− region completely surrounding the n+ implant). But if breakdown is indeed caused by the sharp corners of the base pedestal, the polycrystalline silicon etch process would have to be modified to create more rounded corners.

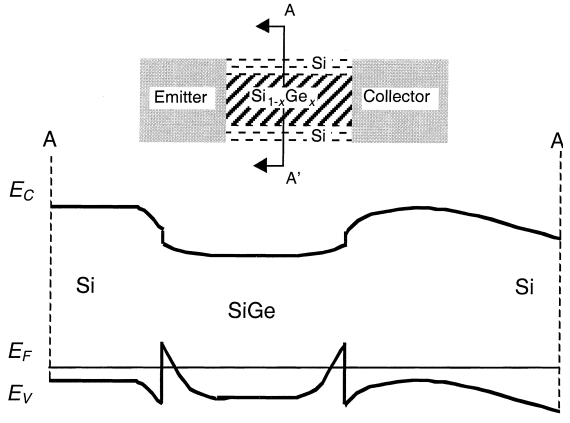

Fig. 10. Band diagram of the Si/SiGe/Si structure used to study carrier confinement in the base of the LBJT [19]. The diagram corresponds to cross section A–A′ in the insert.

4. Future directions

4.1. Silicon-on-insulator

The most natural way of isolating the base of the LBJT, and of confining the carriers to it, is by building it using SOI technology. Along with obviating the need for complex junction-based isolation structures, SOI has the additional advantage of drastically reducing the emitter–substrate and collector–substrate parasitic capacitances, which in turn improves the speed of the device. The most interesting lateral BJTs reported in the literature are built on SOI and offer good performance, provided that the quality of the substrate is good [8,10,12,14].

Several simulations of a NPN LBJT built on a 0.1 μm thick SOI substrate, using uniform emitter and collector profiles, and a horizontal gaussian base profile (uniform vertically), were done to study its performance. Fig. 9 shows the resulting common emitter current gain and cut-off frequency (f_T) (as a function of collector current) for several peak base doping concentrations (N_C), with collector width and doping of $W_C = 0.4$ μm and $N_C = 10^{17}$ cm^{-3}, respectively. The peak cut-off frequency of ~35 GHz for $N_B = 5\times10^{17}$ cm^{-3} is limited by base transit time and is almost an order of magnitude higher than what was obtained for a bulk device. The early voltage for $N_B = 2.5\times10^{17}$ cm^{-3} is 15 V, while for $N_B = 5\times10^{17}$ cm^{-3} it is 18 V.

Gain on the SOI device is obviously very sensitive to surface recombination in the base, on both the base contact and the Si/SiO_2 interfaces. One of the most elegant ways of creating SOI substrates is by Epitaxial Lateral Overgrowth (ELO), which uses a conventional wafer and Selective Epitaxial Growth (SEG) to create islands of crystalline silicon completely surrounded by SiO_2 [18]. This process also results in very good quality Si/SiO_2 interfaces, which minimize leakage currents and recombination. To avoid excessive recombination at the base contact, the Si/polysilicon interface has to be heavily doped (p-type) in order to repel electrons away from it. Diffusion of dopants out of the polysilicon contact automatically creates this heavy doping. At the same time, the height of the base pedestal

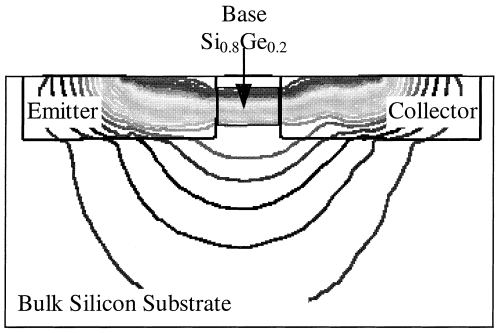

Fig. 11. Simulated current flow-lines in a bulk npn LBJT with a $Si_{0.8}Ge_{0.2}$ channel in the base (compare with Fig. 7).

can be adjusted to increase the distance between the Si/polysilicon interface and the base.

4.2. SiGe heterojunction transistor

An interesting method for carrier confinement in the bulk LBJT is the creation of a SiGe channel connecting the emitter to the collector. Since strained SiGe has a bandgap narrower than that of silicon, most of the carriers will be confined inside the SiGe channel, as is evident from the band diagram in Fig. 10. Even though most of the bandgap difference occurs in the valence band, there is a small step in the conduction band that, along with differences in doping, serves to confine the electrons traveling from emitter to collector [19]. In a device with 20% Ge content in the base ($Si_{0.8}Ge_{0.2}$) most of the electrons are confined to the SiGe channel (see Fig. 11), improving the gain by a factor of two and the peak cutoff frequency by approximately 50% (without any optimization). Unfortunately, most of the holes are still injected into the emitter through its bottom, thus preventing a higher increase of the gain. In spite of the improvements brought about by the SiGe heterostructure, the device still needs some form of isolation which will impact the performance.

5. Conclusions

A lateral bipolar transistor, based on a minimally-modified sub-micron MOSFET, was simulated and fabricated on bulk silicon. The key accomplishments of this work were the following: (1) A novel method of using a base/gate pedestal was used in a self-aligned fashion in conjunction with large-tilt angle, single-sided implants to create asymmetric self-aligned, lightly doped collector regions. These lightly doped regions resulted in the collector-emitter breakdown voltage to increase from 2.8 to 8.0 V. (2) Ideal C–B and C–E junctions were demonstrated with base pedestal contact width of 0.21 μm indicating that the process-induced damage at the edge of the base pedestal was removed by the thermal cycles in the process. (3) Two approaches to solving the problem of loss of carrier confinement were studied by means of simulations: Building the device on Silicon-on-insulator substrates, and introducing SiGe in its base. While the introduction SiGe in the base solves the carrier confinement problem, there are no readily available techniques for fabricating such a structure. On the other hand, the device built on SOI promises very good performance and can take advantage of existing SOI technologies.

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